Characterization of Traps in Acid or Base-Treated GaN Devices

Report by Theodore R. Harris to Doug W. Barlage for ECE633 Independent Study

***Abstract* – GaN MESFETs are promising wide bandgap devices for microwave applications, but are limited by electron-trapping surface states. Groundwork for understanding these devices and issues are presented. This paper reviews previous work to characterize the surface traps in the 1-30GHz range. Current work to passivate the traps by use of strong $K_2S_2O_2$ acid or base is discussed. Circuit configurations are proposed for measurement of electrical characteristics.**

Introduction

Gallium nitride (GaN) metal-semiconductor field effect transistor (MESFET) devices are an area of high interest today as wide bandgap semiconductors. GaN FETs have superior thermal conductivity compared to silicon devices, such that heat capacitance is less of an issue for higher current delivery. They can deliver more current and thus higher power. A further area of improvement is better functionality at higher frequencies. All of these attributes make them ideal candidates for microwave circuits and power amplifiers.

There are currently issues limiting the mass use of GaN transistor devices which affect the key areas of interest already mentioned. Namely, surface states exist at the junctions between different materials due to defects. Depending on the doping material, these traps can be positive or negative. These potential wells introduce nonlinearities in MOSFET devices as AC gate voltages vary with frequency. These surface states cause loss of performance at high frequencies, and degrade current delivery. Ramachandran [1] has shown that the surface states may be characterized electrically.

Vetury [2] describes the surface states acting as virtual gates in which the surface states in the vicinity of the gate trap electrons to act as a negatively charged gate, which must discharge separately. It has been shown that passivated devices do not show current collapse to the same degree. The maximum current deliverable in a microwave measurement is limited by the discharging of the surface state virtual gate. The mechanism for recombination at these sites may be analyzed using Shockley-Reed-Hall kinetics.

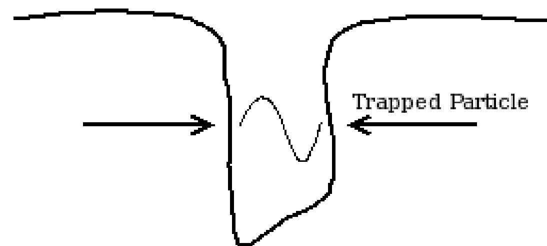

Figure 1. Surface Energy State Trap

The nonlinearities at higher frequencies on the order of 100GHz are a function of the added capacitance of the traps. The effect of the electrons being caught in the traps is that the mobility is reduced. There is a finite probability that the electron will be kicked out of the trap. The Result of this phenomenon is represented below in Figure 3, where an ideal clock signal is applied to the gate. Below, the resultant signal is shown to be distorted. These effects are more pronounced at higher frequencies until the transistor fails to work. V1 is the offset pulse applied to the MESFET gate.

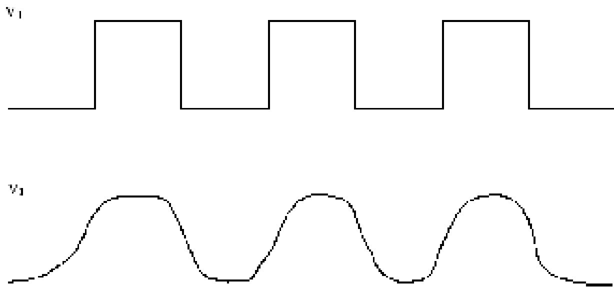

Figure 2. Degradation of Ideal Pulse Train

The traps responsible for this effect reside near the surface of the material, and not within the bulk [1, 5]. The traps in the bulk are not as important to the signal because they can equalize potential much quicker. The material attributes which give rise to the existence of the states can be caused by the following cases. A 2-dimensional atomic representation of a material surface is presented below by Figure 3, with sticks as bonds. Atoms are bound only by one side at the surface, which can leave dangling bonds. This is meant to represent a wurtzite crystal edge where a substitution doping atom changes to silicon.

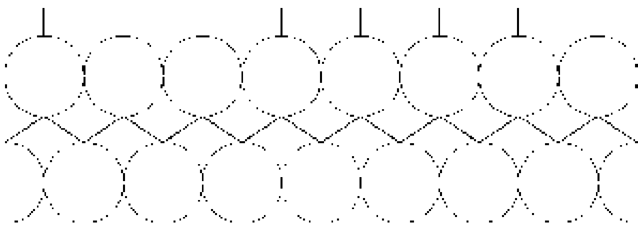

Figure 3. Surface Atoms with Loose Bonds

Along the top of the diagram, unterminated rods, representing loose bonds are visible at the surface (or junction) of the material. These are the features that give rise to the undesired traps which are experimentally removed by a strong acid treatment.

Contaminantory atoms, such as oxide or nitride phases could exist on the surface. Crystal defects inherent to the growth of the bulk may be present near the surface presenting mismatched bonds. Lastly, a mismatch of lattice parameters between the materials will exist at the boundary where the material changes. This change is necessary in the crystal growth to introduce a layer of doping. In this case, the dopant atoms are silicon in the nitride. The (non-surface) traps in the bulk are known as fast traps because they can quickly gain equilibrium with the rest of the bulk, and are of less concern. The surface traps are known as slow traps, whose reluctance to change is detrimental to the usefulness of the device. The classification of traps can be further bifurcated into hole traps, and electron traps, for p, and n-type devices, respectively. The MESFETs discussed in this paper will be understood to be n-channel devices because only n-channel devices have the electron mobility to work in microwave frequencies.

Experimental

The structures fabricated for experimentation by Ramachandra [1] were n-i-n MESFETs. A C-oriented sapphire substrate was used as a base for MOCVD growth of GaN wurtzite layers. The doping was changed during growth to produce intrinsic, p-doped, and then n-doped layers of GaN. Material samples grown at the time of this report by Veety [4] include 300A and 600A thick layers of Si_3N_4 and SiO_2 each. These samples have been pretreated by strong acid to passivate the surface traps. The detail the device fabrication will now be focused on to a further extent. It is important to understand the fabrication and thus structure of the device in order to properly characterize the device behavior.

C-oriented sapphire wafers are immersed in a strong $K_2S_2O_2$ acid bath for passivation, then rinsed in DI water. A layer of Si_3N_4 is grown by MOCVD, and then switched to SiO_2. The PowerFET Mesa mask is used in the first photo-level. Ni is deposited over the photoresist and then lifted off. The Si_3N_4 and SiO_2 are then etched, as an auto-alignment process through the Ni mask. The mesa is then formed by etching. The GaN is deposited, then Ni is etched. The PowerFET Ohmic layer mask is used for the second photo-layer. At this point the sample is

put through an RTA at 850°C. This step introduces some problems and has been reduced to a lower temperature, and may be omitted entirely in the future. The ohmic metal is then removed using another lift-off step. The third photo-level is done using the PowerFET Gate mask. Gate metal is deposited and annealed by RTA. The gate connection to the channel is formed between the drain and source by a Schottky metal contact to the channel. This is different from the ohmic layer, which permits current to flow in either direction, in that it has a rectifying property like a diode. A lift-off step then follows to remove this metal layer. The fourth photo-level uses the PowerFET Interconnect mask. Similarly to the other metal steps, the interconnect metal is deposited and removed by lift-off.

High frequency electrical measurements were made from 1-30GHz. This was done using a Keithley model 4200-SCS probe station and Keithley Interactive Test Environment software. Ongoing at the time of witting, characterization measurements for Veety's samples [4] include drain current, I_d vs V_{ds}, with V_{ds} applied from 0V to 5V at 0.1V increments, and voltage applied to Vg from -5V to 5V in 0.5V increments. The following circuit representation can be used to set up such measurements.

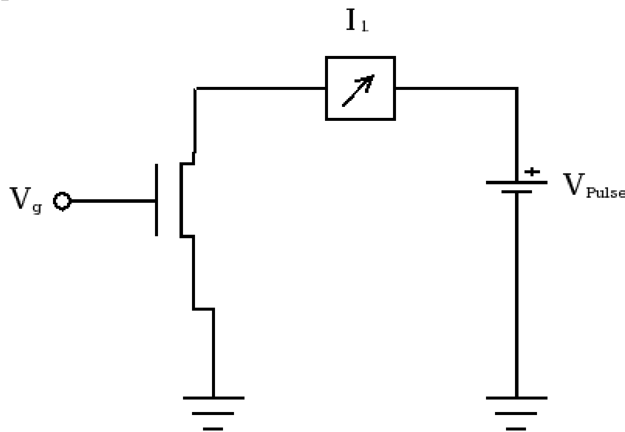

Figure 1. Source Current Measurement

In the above measurement configuration, I_s is measured on a current meter as V_g is varied. The DC voltage supply can change the mode of operation and will vary V_{sd}. The CV curves of the transistors will be measured with the light on and off. This is done with a common source and drain tied to ground while gate voltage is varied from -10V to 10V. The pulsed gate voltages are made with the gate frequency at 800 kHz and 1 MHz. I_d and V_{ds} will be applied at 0.01V and 0.5V increments respectively so that I_d and V_{ds} can be measured with a higher resolution for data collection. Mobility can be calculated by the immediately aforementioned measurements, with higher mobility more desirable, as it reflects proper passivation of traps. To further discuss mobility, recall that in basic terms, mobility can be defined as

$$\mu_n = \frac{q\bar{t}}{m_n *}.$$

With t-bar an amount of time that electrons have not undergone collision, such that a population of unscattered particles in transit across the semiconductor will be related [8]. The population of unscattered electrons should increase as traps are removed.

Another measurement configuration is represented below, in this case allowing a DC offset to the gate with the pulsed measurement on top. Again, source or drain current is measured by the probe station's current meter.

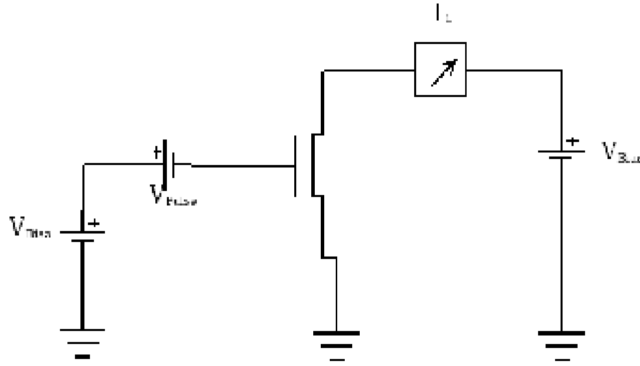

Figure 2. Pulsed Gate Source Current Measurement

These high resolution measurements will be made with the light on and repeated with the light off. A light on the sample can be turned on to fill in the traps so as to subtract the extra capacitance. Ramachandran has shown that capacitance for traps at a single level can be extracted as

$$C_p = C_s + \frac{C_{it}}{1 + (\omega\tau)^2}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau D_{it}}{1 + (\omega\tau)^2} \quad [1].$$

The transconductance of the MESFETs will be measured to further gauge performance. This term will indicate the current deliverable and gain of the MESFET. The set-up for current measurement follows from the basic equation

$$g_m = \frac{dI}{dV_g}.$$

Transconductance, g_m, relates the change in current delivered, dI, to the change in applied gate voltage, V_g. This is measured by varying V_g and finding the ratio, which is dependent of the depletion region, which in turn, is related to frequency. The electron trapping causes a change in g_m at different frequencies. At the lower frequencies, g_m is not an affected to the same degree because the traps are fast enough to follow the changing gate voltage [1 17].

Fowler-Nordheim and direct tunneling are responsible for gate leakage, which will be measured for the devices. The gate leakage current must be subtracted out allowing the drain and source currents to be equal. The extra current found in the source current will be equivalent to the gate leakage in accordance with Kirchhoff's current law.

It is also desirable to measure the pinch-off voltage, V_{PO}, of the fabricated devices. The pinch-off voltage is the voltage applied to the gate where no current flows from the source to the drain, even at high potentials. The channel appears to be an open circuit, but there is residual current which must be taken into account.

Conclusions

The promise of GaN devices has been discussed, including their frequency response, thermal, and power delivery advantages. One of the main limiting barriers to the use of GaN devices is the effect of the surface traps within the GaN material caused by loose bonds. The unpaired bonds trap electrons and reduce mobility and distort frequency response. A plan to model the effect of these traps by pulsed electrical methods has been introduced and discussed. Experimentally, GaN and SiN samples have been treated by strong acid or base to passivate the surfaces. The acid treatment has reduced capacitances and improved signals at high frequencies. The approaches to electrically characterizing transistors have been introduced, and measurement configurations have been suggested. Future work includes using scattering parameters to accurately model high frequency effects observed, and to eliminate any undesirable non-linearities. All of these improvements will be possible through further fabrication experiments to improve material quality.

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