Comparative Analysis of 22nm Gate Length Silicon nMOS Device to $In_{1-x}Ga_xAs$

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Abstract — **Many electrical engineers agree that the end of Moore's Law could be fast approaching for the industry standard Si. One obvious solution to this problem is to move to new, novel materials. GaAs and InGaAs are of interest due to their high electron mobility, and are investigated in this study. The electrical properties of GaAs and InGaAs are contrasted to a Si device adhering to the ITRS 2008 road map using the Isetcad software package.**

***Index Terms*—high K dielectric, InGaAs, GaAs, 22nm gate length, short channel devices, MOSFET.**

I. Introduction

Other types of transistors are sometimes preferred in the case of InGaAs, such as MESFETS, and the JFET in order to increase mobility. In this case it is desirable to directly compare similar devices in Si and InGaAs, therefore the ITRS 2008 road map will be followed. The following dimensions were chosen based on the ITRS; a gate length of 22nm, an effective oxide thickness of 0.8nm ($Si0_2$), spacer width of 9nm, source/drain junction depth of 20nm, and a source/drain extension junction depth of 5nm. The Doping levels of the drain source doping are 1e21 cm^-3 (peak), 1e18 cm^-3 (Junction), with a lateral factor of 0.8. Arsenide was used as a dopant in the software, simulating an accepter dopant. In actual devices, groups II and VI are potential dopants. Si, Be, C, and even the transition metal Zn are proposed dopants for InGaAs and GaAs. The alternate doping issue in the software is discussed in more detail in the *DESSIS Configuration* section. The fact that hole mobility is very poor in p-type InGaAs materials worsens its extension to CMOS technology.

Arguably the worst problem concerning the move to a GaAs technology is surrounding the high-K gate dielectric needed. HfO_2 is one promising dielectric which can be grown by atomic layer deposition on GaAs.[1] In this case, K is taken to be 21. Electron mobility can actually be decreased in the bulk by addition of high-k dielectrics, due to the fact that the GaAs poor surface on which to grow oxide. There is a crystal lattice mismatch between the dielectric and the substrate, and the surface plane may intersect with the As atoms in some locations. The loose bonds create undesired interface states, which cause scattering and lower mobility.

Another significant design challenge is the fact that most metals have a very low Schottky barrier height of approximately 0.2eV to InGaAs. [3] It is important to note that metal contact to InGaAs have not been considered in this study. Typical metal work functions of Si were also used for InGaAs of 4.05eV. The metal gate - HfO_2 interface is also critical to understanding the electrical behavior of MOS devices. Fermi level pinning is a phenomenon that occurs at metal – dielectric interfaces which causes undesirable shifts in the effective metal work function. Schaeffer *et all* have all found that electrodes comprised of weak oxide forming transition metals demonstrate a propensity to inter-diffuse through the poly-crystalline HfO_2 dielectric. [2]

Making smaller devices inherently requires smaller gate length. A smaller gate length presents many challenges in the device design arising from the presence of short channel effects. In order to maintain gate control of the channel, oxide thickness must be scaled down to increase the effective gate to channel capacitance. A higher C_{GC} implies that for a given increase in gate voltage, more charge appears in the channel. The necessity of a smaller oxide thickness gives rise to higher gate leakage. [3] One solution to mitigate gate leakage is the use of high-K dielectrics which can have a larger thickness but have the same effective Cox as a much thinner SiO_2 layer.

However, the use of high-K dielectrics for MOSFETs reduces bulk mobility in Silicon. To counter this effect, alternate semiconductors with higher mobility must be used for the substrate. GaAs is one such material favored for its higher velocity saturation and higher mobility. [4] Silicon's electron mobility of 1350 cm^2/Vs is lower than the 8500 cm^2/Vs of GaAs. Variable molefractions of Indium in the compound InGaAs can increase the mobility to an upper limit of 22600 cm^2/Vs, belonging to InAs. [5]

Indium Arsenide alone is not a useful material to be used as a MOSFET substrate. However, including Gallium in InAs allows the material's bandgap to be scaled with Ga concentration. An increase in bandgap will be shown to cause both Ioff and Ion decrease. Thus, varying the mole fractions of In and Ga allows some flexibility in designing for subthreshold slope and extrapolated threshold voltage. With the InGaAs substrate, we were able to design a device with off-state current equivalent to the core device but with higher on-state current.

II. Procedure

A. General Approach

The purpose of this project was to compare Si to compound semiconductors with a higher and lower bandgap. This was accomplished using InGaAs, since this ternary alloy's bandgap can be raised and lowered with appropriate In–Ga mole fraction. Through appropriate simulations, the Id, Vg curves for varying mole fractions could be compared to the Id,Vg curves for the Si-bulk MOSFET.

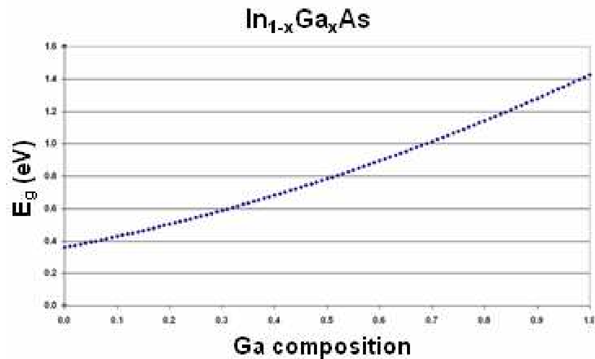

Figure 1 – High V_{DS}=1V InGaAs, Optimum refers to $In_{0.9}Ga_{0.91}As$

First we developed a core device using a Si substrate to meet the design specifications of I_{off} = 1µA/µm and an I_{on} of 1mA/µm with an equivalent oxide thickness (E0T),with respect to $Si0_2$ of 0.8nm. The parameters of core, GaAs, and $In_{0.9}Ga_{0.91}As$ devices are listed in Table 1. We then altered the core device model to have a GaAs substrate and $In_{1-x}Ga_xAs$ substrate with differing mole fractions. We then characterized each device and compared their performance using various data, such as Id vs Vds curves, Id vs Vgs curves, subthreshold slopes, and their on and off-state current values. More specific details of the procedure for modeling each material system are found below.

B. Core Device

In order to meet the design specifications for the core device using a Silicon substrate, a 2-D MOSFET was modeled in ISE TCAD. The structure's boundary and doping were defined using MDRAW, a device modeling software. Using an L_{drawn} of 22nm, we varied multiple device parameters until the desired I_{on} and I_{off} values were achieved. During this process, we noticed various trends that ultimately led to the final core device design. We determined that changes in the source/drain extension width result in the most significant shifts of I_{on} and I_{off}. Decreases in the source/drain extension widths result in increases in both I_{on} and I_{off}, with the most noticeable impact being the increase in I_{off}. Conversely, source/drain extension depth had a minimal impact on the values of I_{on} and I_{off}. Furthermore, higher substrate dopings minimized I_{off} at the expense I_{on}.

Using these trends, we were able to decrease I_{off} by a large amount through a slight increase in substrate doping. Left with an unsatisfactory I_{on}, junction depth was slowly increased while extension depth remained constant. Increasing the source/drain junction depth had a much greater effect on I_{on} than I_{off}, allowing the core device's specifications to be met.

TABLE 1
DOPING SUMMARY

Param	Core (Si)	In(0.09)Ga(0.91)As	GaAs
Leff	20.8 nm	20.8 nm	20.8 nm
High-K (εr)	21	21	21
Tox	4.3 nm	4.3 nm	4.3 nm
EOT (SiO2)	0.8 nm	0.8 nm	0.8nm
Extension Depth	5 nm	5 nm	5 nm
Extension Doping	$1x10^{18}$ cm^{-3}	$1x10^{18}$ cm^{-3}	$1x10^{18}$ cm^{-3}
Junction Depth	20 nm	20 nm	20 nm
Junction Doping	$1x10^{21}$ cm^{-3}	$1x10^{21}$ cm^{-3}	$1x10^{21}$ cm^{-3}
Φms	4.05 eV	4.05 eV	4.05 eV
Substrate Doping	$3x10^{18}$ cm^{-3}	$3x10^{18}$ cm^{-3}	$3x10^{18}$ cm^{-3}
Vdd	1V	1V	1V

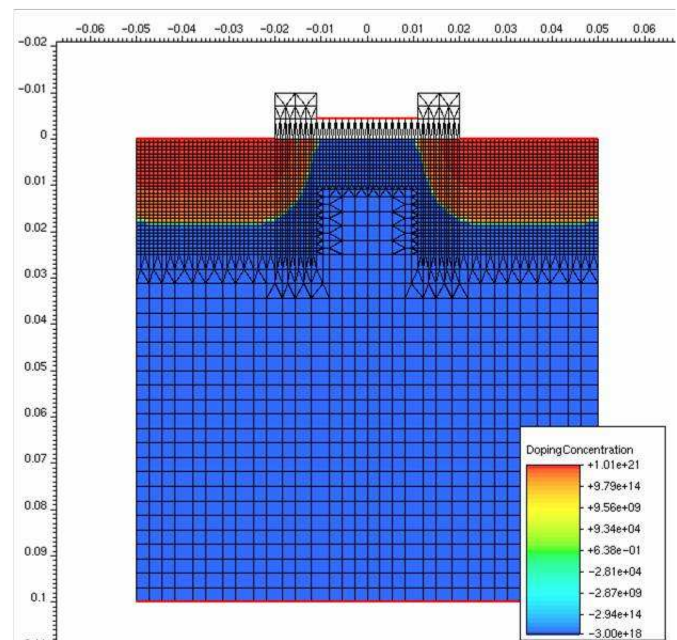

Figure. 2. Cross-section of MDRAW device showing grid density

Due to the short channel length of the device, a small effective oxide thickness (EOT) of SiO_2 is needed to maintain gate control of the channel. The requirement for the EOT of for the device is 0.8nm. However, at such small dimensions, a thicker physical gate oxide is needed to prevent the large gate leakage currents that result from an $Si0_2$ gate oxide of 0.8nm physical thickness. The insulator was chosen to be of an arbitrary material known as "Insulator 1," in the ISE TCAD layout tool, MDRAW. We defined a special DESSIS parameter file for Insulator1 to reflect a new permittivity of 21 as opposed to its default value of 3.9 (SiO_2). The physical thickness of this layer gate oxide layer was 4.3nm for an EOT

of 0.8 nm. This allowed our simulation to emulate a high relative permittivity that is physically attainable with HfO_2.

With the core device defined, it was then meshed in MDRAW to create the appropriate files needed to properly simulate the device. *Fig. 1* shows the meshed core device and its doping concentrations.

With the Si core device defined in MDRAW, we performed simulations on the device by running three DESSIS command files. The first DESSIS command file created Id vs Vgs curves for a high Vds value, 1V. The second DESSIS command file created Id vs Vgs curves for a low Vds value of 0.125V. These voltages were selected based on the fact that Vdd=1V and that the Id vs Vgs curves would not converge for the GaAs and InGaAs devices for a Vds value of less that 0.125V. The third DESSIS command file created an Id vs Vd curve for five values of Vgs(0V. 0.25V, 0.5V, 0.75V, 1V). These curves were then viewed in Inspect. The core device was left intact for the remainder of this investigation.

C. GaAs and InGaAs

Using the infrastructure of the core device, the material of the substrate was changed to GaAs in MDRAW. All other parameters of the device were unchanged. The devices were then renamed and meshed to create the proper input files for the simulation. Additionally, we generated a parameter file for GaAs using DESSIS to provide the DESSIS simulation engine with the appropriate physical parameters for GaAs, such as bandgap, permittivity, carrier mobility, and many other complex parameters of the material. The three DESSIS command files were then modified to include the appropriate boundary, doping profiles, and parameter files for the GaAs device. We simulated the three command files, and obtained the Id vs Vgs curves for high and low Vds values, as well as the Id vs Vds curves.

For $In_{1-x}Ga_xAs$, the same basic procedure was followed. The MDRAW model core device was modified to have an InGaAs substrate. All doping profiles were unchanged. The parameter file was then generated for InGaAs in the same manner as was done for the GaAs device. The command files were then edited to include appropriate boundary, doping, and parameter files.

The main difference in the procedure for the GaAs and InGaAs devices was the inclusion of a mole fraction term in the Physics section of the InGaAs command files. This allowed for variance of the mole fraction, x, and extraction of differing curves for different mole fractions of $In_{1-x}Ga_xAs$. The InGaAs devices were then simulated for various mole fractions and their performance was compared based on the Id vs Vgs curves. Further details of how DESSIS manages the mole fraction term are provided in section *D*.

D. DESSIS Configuration

Because the accuracy of the simulations depends heavily on the accuracy of the parameter file being used for materials other than Si, the default parameter file, it was decided to use GaAs and InGaAs instead of GaN and InGaN. It was then found that GaN and InGaN do not have parameters that are well defined within ISE TCAD. We attempted to generate an acceptable parameter file for GaN, however, the results from simulation were highly inaccurate due to the simplicity of the model we were able to develop on our own.

Another issue with DESSIS is that alternative dopants are not well supported in ISE TCAD. In the command files, an As analytical doping was used for the n-type regions and B for the p-type regions for the core (Si), GaAs, and $In_{0.9}Ga_{0.91}As$ device. In real word devices, InGaAs in most commonly doped p-type with Zn and n-type with Silicon.[3,4]. Similarly common dopants for GaAs are Be for p-type and Si for n-type GaAs.

According to the DESSIS manual, "DESSIS supports the most important dopants used in silicon technology: the donors As, P, Sb, N, and the acceptors B and In. For the simulation of other semiconductors such as III–V compounds, the actual dopants (such as Si and Be) are supported only through user-defined species." We were not able to appropriately define the dopant species in the correct file such that we could use alternate dopants. Also, there is no mechanism within MDRAW to specify a user defined dopant in the doping profile. As a result, we left as ArsenicActiveConcentration for n-type regions and BoronActiveConcentration for p-type regions.

One important aspect of simulation is the method by which DESSIS determines the appropriate material parameters for the $In_{(1-x)}Ga_xAs$. According to the parameter file for InGaAs, the material parameters are determined via a linear interpolation between the materials parameters of InAs and GaAs. In our case when x=1, using the MDRAW file for InGaAs, the material behaves as GaAs. We verified that the Id vs. Vds and Id vs. Vgs curves for GaAs exactly matched those generated when the MDRAW files containing the InGaAs substrate were simulated using a mole fraction of 1.

III. Results And Analysis

A. Id, Vg

The core Silicon device displayed the highest off-state current and lowest on-state current, as summarized in *table 2*. $In_{0.9}Ga_{0.91}As$ was chosen for its ability to match the core device's I_{off}, which also resulted in a 29% increase of I_{on}. GaAs exhibited an off-state current almost an order of magnitude lower than both of the previous substrate materials.

TABLE 2
ION / IOFF

Material	Ion	Ioff
Si	1.14 mA	965 nA
InGaAs	1.47 mA	939 nA
GaAs	1.27 mA	115 nA

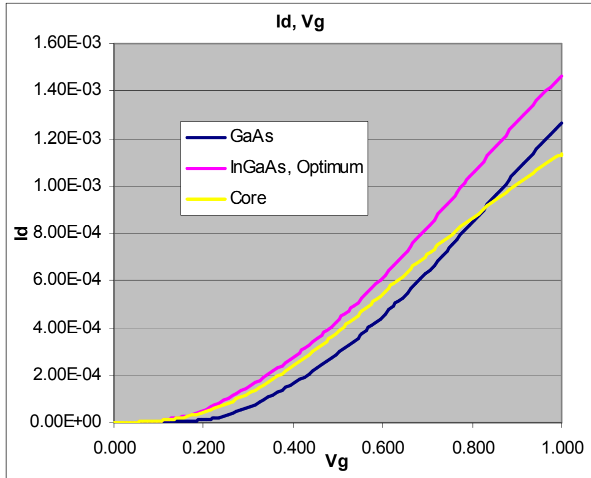

Figure 3 – High V_{DS}=1V InGaAs, Optimum refers to $In_{0.9}Ga_{0.91}As$

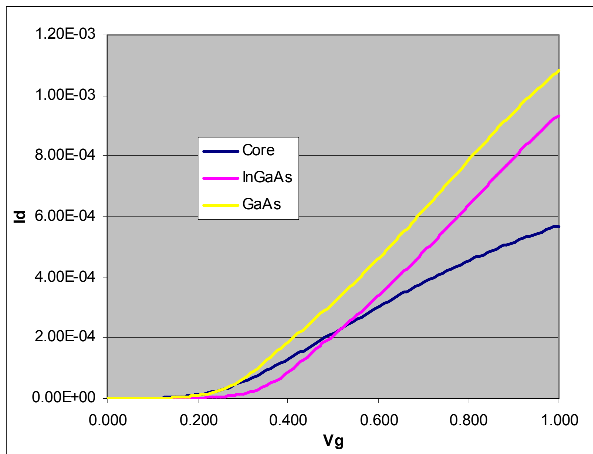

Figure 4 – Id, Vg for V_{DS} =0.125V

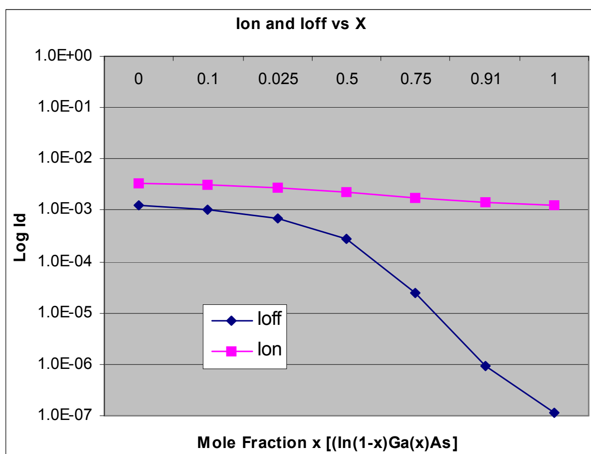

Figure 5

B. *Subthreshold Slope*

The slope of the ln(Id) vs Vg was calculated for both high and low values of V_{DS}. Using the inverse of the slope, the subthreshold slope, S, was found. In both cases, the GaAs device exhibits the smallest, most desirable value of S. There is a difference between the S values for the Vds=1V and Vds=0.125V. The values of S are higher for higher values of Vds. This difference corresponds with the presence of drain induced barrier lowering (DIBL).

TABLE 3
SUBTHRESHOLD SLOPE

Material	Vds=0.125V	Vds=1V
Si	85 mV/decade	104.6 mV/decade
InGaAs	85 mV/decade	104.6 mV/decade
GaAs	84 mV/decade	94.6 mV/decade

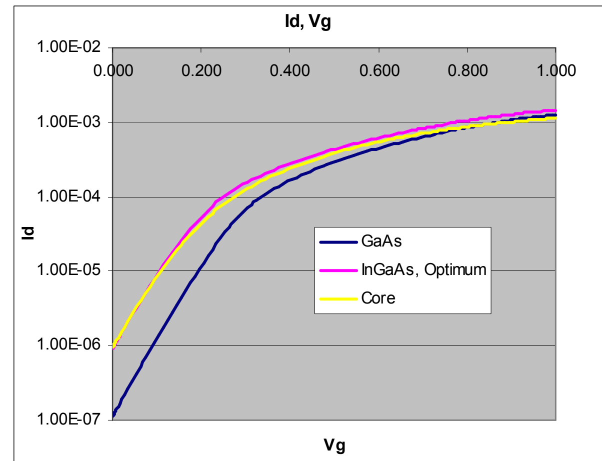

Figure 6 – Id, Vg for V_{DS} =1V

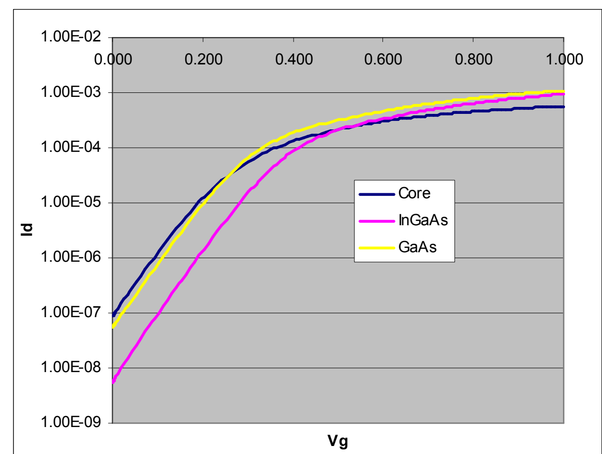

Figure 7 – Id, Vg for V_{DS} =0.125V

TABLE 4
EXTRAPOLATED THRESHOLD VOLTAGE

Material	V_T
Si	266.5 mV
InGaAs	309.0 mV
GaAs	383.4 mV

Calculated from Id, Vg curves for high V_{DS} See appendix for curves.

All curves display the presence of velocity saturation for each of the three devices. From long-channel theory, in the absence of velocity saturation the saturated regions should have a square-dependence on $V_{eff} = V_{GS} - V_T$. In other words, the ratio between two effective voltages and two corresponding drain currents in the saturation region should be roughly Id_1 / Id_2 = ($V_{eff,1}$ / $V_{eff,2}$)^2.

Ideally, the drain current at Vg=0.5 for each MOSFET should equal the drain current at Vg=0.25 multiplied by the squared ratio of the effective gate voltages. This can also be done for a gate voltage of 1V. A measure of this predicted drain current can be compared to the simulated drain current to give an indicator of velocity saturation.

With V_D held constant at 1V, the expected Core drain current at Vg=0.75V from the current at Vg=0.5V is approximately 1.642 mA. Compared to the simulations which showed I_D=789uA, there is a 52% error. A similar analysis was done for the GaAs and InGaAs MOSFETS, which had experimental errors of 74.5% and 59.2%, respectively. Such large errors lead to the conclusion that all three suffer from velocity saturation.

C. Id, Vd Family of Curves

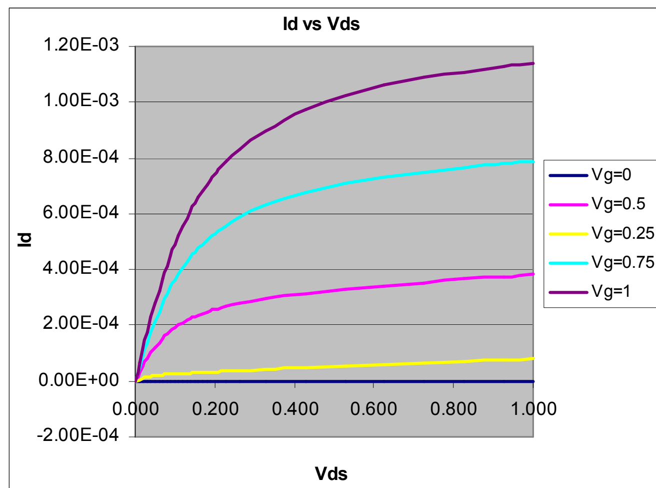

Figure 8 – Core device

The Id, Vd curves for GaAs and InGaAs contain noticeable discontinuities at each transition region from triode to saturation. This possibly results from the simulator switching between two equations that have been tailored to properly agree for a Si substrate. The modification to alternative bulk materials coupled with high horizontal electric fields must be producing unmanageable effects from channel length modulation. Refining the meshes and minimizing the simulation's voltage steps were not effective in mitigating this problem.

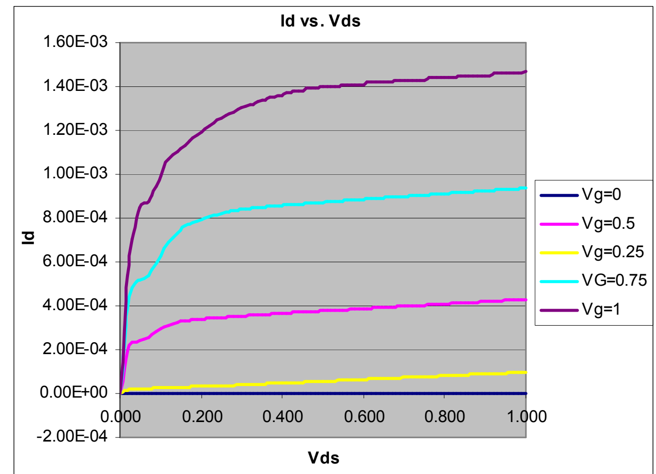

Figure 9 - $In_{0.9}Ga_{0.91}As$

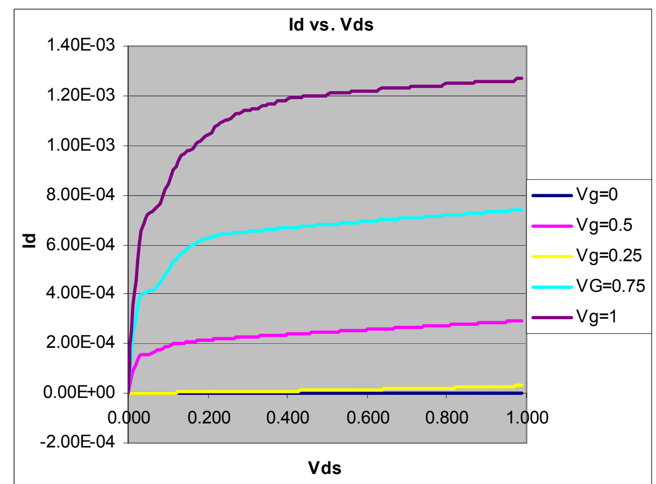

Figure 10 - GaAs

IV. CONCLUSION

A working GaAs device was simulated and outperforms the Si core devices due to its increased mobility. An $In_{1-x}Ga_xAs$ device was designed to properly function within the constraints.

It is not convincing that GaAs or InGaAs devices will soon if ever replace the established Si technology. The most significant drawbacks include metal gate contacts, and growing a suitable high-k dielectric.

The strategy of combining short-channel MOSFETs with the use of a high-K dielectric allows the realization of high drive current minus the gate leakage present in a classical SiO2 dielectric layer. Further advances can be made with high-mobility bulk materials whose characteristics such as bandgap and mobility have a direct influence on Ion and Ioff.

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