

Objective

To obtain a full-time position related to computer architecture.

Research Interests

High performance microarchitecture, cycle-level processor simulation tools, instruction-level parallelism, improving single-thread performance using novel microarchitectural techniques, heterogeneous multi-core design, trace-level reuse.

Education

North Carolina State University Ph.D. , Computer Engineering (GPA: 4.0/4.0) Advisor: Dr. Eric Rotenberg	Raleigh, NC <i>Aug 2006 - May 2012 (Expected)</i>
Temple University M.S.E. , Electrical Engineering (GPA: 3.97/4.0) Thesis: Reducing the overhead of Runahead Execution using RENO	Philadelphia, PA <i>Aug 2003 - May 2006</i>
University of Mumbai B.E. , Electronics Engineering	Mumbai, India <i>Sep 1999 - June 2003</i>

Publications

FabScalar: Composing Synthesizable RTL Designs of Arbitrary Cores within a Canonical Superscalar Template. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Hiran Mayukh, Jayneel Gandhi, Brandon Dwiell, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *IEEE Micro Top Picks*, Issue 3, May-June 2012 (To appear).

FabScalar: Composing Synthesizable RTL Designs of Arbitrary Cores within a Canonical Superscalar Template. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Hiran Mayukh, Jayneel Gandhi, Brandon Dwiell, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *International Symposium on Computer Architecture*, June 2011.

FabScalar. Niket K. Choudhary, **Salil Wadhavkar**, Tanmay Shah, Sandeep Navada, Hashem H. Najaf-abadi, and Eric Rotenberg. *Workshop on Architectural Research Prototyping (WARP)*, held in conjunction with ISCA-36, June 2009.

Current Research

Choosing cores for robust heterogeneous multi-cores: Single ISA heterogeneous multi-cores offer a promising approach for designing future multi-cores. Given the application diversity in today's systems, a multi-core can be composed of cores designed to cater to different application characteristics. This research investigates methods to recommend a set of core designs that offer close to optimal performance for a wide range of applications by studying common application characteristics and processor resource requirements. A set of such diverse cores eliminates the need to design a per-application optimal core from scratch using time-consuming design space explorations.

Past Research

Framework for Processor Customization and Design-Space Exploration: A detailed cycle-accurate simulation framework to model a customizable RTL (Verilog) model of a superscalar processor was developed using C++. This framework can be used wherever fast and accurate estimate of performance is needed, for example, the design-space exploration of a superscalar processor, pre-RTL evaluation of microarchitectural techniques, etc.

Partial trace-level reuse: Trace-level reuse eliminates the need to execute complete sequences of instructions by matching the trace inputs with previously stored instances. However, this requires a large amount of storage to be effective. This research optimized general trace-level reuse by identifying that dependence chains are more suitable for reuse due to the dataflow relationship among instructions.

Work Experience

Intel Corp. , Software Services Group Performance Tools Intern Ported SEP, a performance profiling tool, to support heterogeneous processor platforms. Investigated techniques to improve resource utilization of SPEC benchmark suites on heterogeneous processor platforms.	Santa Clara, CA <i>Feb 2011 - Aug 2011</i>
North Carolina State University , Dept. of Electrical and Computer Engg. Research Assistant	Raleigh, NC <i>Aug 2007 - Present</i>
North Carolina State University , Dept. of Electrical and Computer Engg. Teaching Assistant	Raleigh, NC <i>Aug 2006 - Aug 2007</i>
University of Pennsylvania , Dept. of Computer and Information Science Research Assistant	Philadelphia, PA <i>Jun 2006 - July 2006</i>
Temple University , Dept. of Electrical Engg. Teaching, Research Assistant	Philadelphia, PA <i>Jun 2004 - May 2006</i>

Selected Academic Projects

Long Latency Cache Miss Tolerant Architectures: A comprehensive evaluation and comparison of L2 cache miss latency tolerant techniques such as Runahead Execution, Checkpointed Early Load Retirement, and Continual Flow Pipelines, on a ROB-based dynamically scheduled superscalar substrate. *2007.*

Smart Victim Cache: Improving the performance of a victim cache by selectively allocating and replacing cache blocks. *2007.*

MiniC Compiler: A VLIW compiler for MiniC that performs scheduling and employs well-known back-end optimizations. *2007.*

UNIX Thread Library: A user-level thread library, similar to the POSIX thread library, including a preemptive round-robin scheduler and synchronization primitives. *2007.*

Mutual Exclusion in Distributed Systems: A library for ensuring mutual exclusion between processes, using an optimized version of the Lamport algorithm. *2007.*

Profiling and Timing Analysis for Embedded Systems: A study of application behavior and code timing analysis for embedded systems using the M16C microcontroller. *2007.*

RTOS Instrumentation: A study of μ C/OS-II real-time operating systems using instrumentation code and transmitting data on the serial port to represent system events. *2007.*

Thread-Level Speculation on Multi-core Processors: A detailed memory-side simulator extension for exploiting Thread-Level Speculation in Chip Multi-Processors. *2006.*

Benchmark Study for Thread-Level Speculation: A run-time and code-level analysis of a floating-point benchmark `equake`, to identify opportunities for exploiting Thread-Level Speculation. *2006.*

MSI Implementation: An implementation of the MSI cache coherence protocol for parallel processors using SESC. *2006.*

Technical Skills

Simulator development, C/C++, Assembly, Verilog HDL, BASH, Perl, Cadence Tools (Schematic and Layout) \LaTeX , Linux, Windows.

Professional Affiliations

Student Member - IEEE, ACM-SIGARCH
Member - Phi Kappa Phi