AnyCore-1: A Comprehensively Adaptive 4-Way Superscalar Processor
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AnyCore-1

- A comprehensively adaptive out-of-order superscalar core which adapts to the available ILP in programs.
- Dynamically changes superscalar width and sizes of ILP extracting structures.
- Orthogonal to DVFS and can improve energy efficiency further.
- To the best of our knowledge, AnyCore-1 is the first adaptive processor chip.

Key Results
- Power consumption and IPC scale with configured core size.
- Idle power is large due to clock tree and fully synthesized caches.
- Currently we are trying to run SPEC 2000 SimPoints on AnyCore.

AnyCore-1 Chip Details
- Fabricated in 130nm technology.
- Clock gating at level of lanes and structure partitions.
- Input gating of de-configured ports.
- CQFP-100 package (79 signal pads, 21 power pads).

Test Infrastructure
- Xilinx ML-605 board used as a testbench.
- Custom mezzanine card interfaces chip to ML605.
- L2 Controller in FPGA (currently uses block RAMs).
- FPGA talks to AnyCore-1 through a Management Bus.

Table: Physical Design Information

<table>
<thead>
<tr>
<th>Physical Design Information</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>IBM 8RF (130nm)</td>
</tr>
<tr>
<td>Dimensions</td>
<td>5 mm x 5 mm</td>
</tr>
<tr>
<td>Pads (Signal, Power)</td>
<td>100 (79, 21)</td>
</tr>
<tr>
<td>Transistors</td>
<td>3.4 million</td>
</tr>
<tr>
<td>Cells</td>
<td>1.5 million</td>
</tr>
<tr>
<td>Nets</td>
<td>7.4 million</td>
</tr>
</tbody>
</table>

Power

<table>
<thead>
<tr>
<th>Power Configuration</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leakage Power</td>
<td>0.01</td>
</tr>
<tr>
<td>Idle Power</td>
<td>21</td>
</tr>
<tr>
<td>Idle Power</td>
<td>25</td>
</tr>
</tbody>
</table>

AnyCore-1 Microarchitecture

Reconfiguring AnyCore-1
- Reconfiguration penalty is ~20 cycles.
- Reconfiguration can take up to 150 cycles.
- Three ways to trigger reconfiguration in our test setup.
  1) By the program, by issuing a store with the configuration to a reserved memory location.
  2) By the testbench hardware based on performance counter driven bottleneck analysis.
  3) By the console program based on scheduling constraints.

Experiments with AnyCore-1
- AnyCore-1 successfully runs many different microbenchmarks, with dynamic reconfiguration enabled and disabled.
- Currently we are trying to run SPEC 2000 SimPoints on AnyCore-1.

Table: Benchmark Details

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Dynamic Instr. (million)</th>
<th>Avg. IPC</th>
<th>Avg. Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reduce an array to a sum</td>
<td>235.46</td>
<td>3.05</td>
<td>36.25</td>
</tr>
<tr>
<td>Bubble sort an array</td>
<td>36.52</td>
<td>0.32</td>
<td>27.50</td>
</tr>
<tr>
<td>Prime Number Generator</td>
<td>38.28</td>
<td>1.52</td>
<td>30.63</td>
</tr>
<tr>
<td>Linear Feedback Shift Register</td>
<td>67.11</td>
<td>1.57</td>
<td>30.63</td>
</tr>
<tr>
<td>Sum first N natural numbers</td>
<td>67.11</td>
<td>4.00</td>
<td>36.25</td>
</tr>
</tbody>
</table>

Adaptive Core vs. Fixed Cores
- Scheduler adjusts configuration for each program phase to minimize energy while maintaining close to maximum performance for the phase.
- Dynamic reconfiguration at phase boundaries places AnyCore-1 at the pareto frontier.
- AnyCore-1 enables the scheduler to trade performance for lower energy.

AnyCore 4-Way Superscalar Processor

AnyCore RTL Design
- A synthesizable parameterized RTL design of an adaptive superscalar core.
- Can generate both adaptive and fixed cores of arbitrary maximum size.
- The RTL is paired with UPF based power domain description for power gating of lanes and partitions.

AnyCore CAD Flow
- Industry-standard synthesis and analysis flow to easily quantify circuit-level overheads.
- Clock gating and power gating methodology to maximize power savings from disabled resources.

AnyCore PAT Tool
- A Power-Area-Timing database generation tool that can be coupled with C++ based microarchitecture simulators for broad exploration studies.
- Automatically synthesizes, analyzes, and populate PAT database – easy to use for computer architects who are not familiar with low-level flows.
- Uses UPF-based per-domain power analysis to populate power database.

Enables Adaptive Core Research
- Understand circuit-level overheads of adaptivity.
- Compare comprehensively adaptive cores with other adaptive architectures such as heterogeneous multicores.
- Fabricate adaptive superscalar cores like AnyCore-1.

References

Hot Chips 28, 21 – 23 August, 2016, Cupertino, California, USA
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