

Niket Kumar Choudhary

Contact

E-mail: niket.chy@gmail.com

Phone No. (845) 337-6468

2300, Avent Ferry Road, Apt-K2

Raleigh, NC, USA 27606

Objective

To seek a coop/intern position in the area of computer architecture.

Education

M.S. – Thesis in Computer Engineering: (Aug, 2007 – present)

North Carolina State University, Raleigh, NC

GPA: 4.0/4.0

Advisor: Dr. Eric Rotenberg

B.Technology in Information & Communication Technology: (Aug, 2001-May, 2005)

Dhirubhai Ambani Institute of Information and Communication Technology, India

Experience

1. Research Assistant at North Carolina State University, NC, USA (Aug, 2007 – present)

I am working towards advance computer architecture under Dr. Eric Rotenberg. Currently I am building synthesizable model (Verilog) of a superscalar microarchitecture similar in complexity to modern processors.

This model will be used for exploring low-power, complexity effective and fault tolerance on a superscalar processor. The model will also be used for exploring heterogeneous chip-multiprocessor design.

Design Engineer at ARM Private Ltd, Bangalore, India (Aug, 2005 – July, 2007)

I worked for Processor Division group where my primary responsibilities had been development of low power techniques (architecture and block level) for ARM processors and their VLSI implementation. Following are major projects I had been involved:

- § Co-developed Intelligent Energy Management (IEM) solution for ARM1176JZF-S processors using Cadence digital IC products. ARM's IEM solution is based on the concept of DVFS to achieve greater energy savings in a CPU core by optimally balancing processor workload and energy consumption. The work involved low power micro-architecture development, partitioning design in appropriate power domains, deploying synchronous/asynchronous AXI interface for L2 instruction and data cache, direct memory access, and peripherals.
- § Developed automatic test pattern generation (ATPG) flow for ARM leading processor using Cadence's Encounter Test tool. It encompassed stuck-at faults, bridging faults, and delay faults in a circuit.
- § Done benchmarking of multiple ARM processors for power, performance, and area targeted to different CMOS technologies (130, 90, & 65nm) using Cadence and Synopsys digital products. These figures are used by ARM for product marketing.

3. Intern at Cadence Design System, Bangalore, India (Jan, 2005 – May, 2005)

I worked in the logic synthesis group at Cadence where I learnt various CAD related challenges for deep submicron SoC designs. Responsibilities included:

- § Developed solutions for efficient and accurate synthesis of high performance floating point datapath based on IEEE 754 standard.
- § Contributed in solving implementation related issues like multi-threshold implementation, high performance datapath synthesis for Cadence's customers.

Technical Skills

Professional Tools	<i>Cadence</i> (NC-Verilog, RTL Compiler, SOC Encounter, Encounter Test, Celtic NDC, Voltage Storm, Fire & Ice, Virtuoso), <i>Synopsys</i> (Design Compiler, PrimeTime), MATLAB
Simulators	GEMS, SimpleScalar
Programming Language	C, C++, Verilog
Scripting Language	TCL, Perl, Shell Script
Competencies	Computer Architecture, Digital design, RTL Coding, ASIC Flow

Papers

1. **Niket Choudhary** and Giorgio Parpani. "ARM IEM Implementation with Cadence Digital IC Products", at Cadence symposium, Bangalore, India, October 2006.
2. A. Bhatt, C. Sachdeva, M.Desai., **N Choudhary**, S. Chouksey, Y. Bansal., T. Ahmed, and T. Abbasi. "32 bit RISC Pipelined Processor," ICON Cadence India Newsletter, February 2005.
3. A. Bhatt , **N.Choudahry** and S.Chouksey. "A Novel Algorithm for Software Scheduling and Methods to Reduce Stalls in RISC Pipelined Processor," Malaysia Region 10 Contest, 2004.

Relevant Courses

Computer Design & Technology	Parallel Computer Architecture	Computer Architecture
Advance Parallel Computer Arch	Digital ASIC Design	VLSI Systems Design
Code Generation and Optimization	Internet Protocols	

University Projects (Relevant)

1. Implementation of Owner and Sharer predictors in Simultaneous Multiprocessing environment on MOESI protocol using GEMS package in Simics.
2. Implementation of RegionScout Mechanism on MOSI protocol using GEMS package in Simics.
3. Implemented a superscalar pipeline simulator based on Tomasulo's algorithm.
4. Implemented L1 and L2 data cache simulator for different write policies for characterizing memory behavior.
5. Implemented branch predictor simulator for characterizing branch behavior.
6. RTL implementation of regular expression matching hardware.
7. Designed and implemented reduced version of an Orthogonal Frequency Division Multiplexing (OFDM) system using Cadence ASIC tools. Most of the system specifications were derived from 802.11a wireless LAN protocol.
8. Custom VLSI Implementation of Binary Search Algorithm (Schematic Design to Final Layout) using LTspice, Magic and Irsim tools.

Honors and Achievements

1. Member National Scholars Honor Society
2. IEEE student member
3. Chairman IEEE student branch, DAIICT (2004)