

A Novel Design Procedure for Tunable Low Noise Amplifiers

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Abstract

A novel design methodology for tunable low noise amplifiers with the associated circuit topology will be presented. The procedure steps based on low noise design essentials are given as the main results of their mathematical analysis using the circuit and noise theory. After the methodology is demonstrated at narrowband by the simulation graphs, the tunability aspect of the design using the series matching at the input and output will be verified. If a tunable capacitor is inserted to the base of the heterojunction bipolar transistor (HBT) at the input, simulation outcomes reveal that for the range of 3.5- 6.5 GHz, input and output return ratios (S_{11} and S_{22}) can be ensured to be below -10 dB and the difference between noise figure (NF) and minimum noise figure (NF_{MIN}) to be below 0.5 dB.

1. Introduction

Low noise amplifiers (LNAs) constitute the first stage of the conventional receiver systems and should be built for low noise figure and high gain. Various design procedures have been put forward to realize the specifications of LNAs imposed by the wireless communication systems [1]-[4]. Different circuit techniques were considered to achieve input and noise power matching at the same time such as an inductor in the source (emitter) [1]-[4] or an additional gate-source (base-emitter) capacitance [3], [4]. The widths (emitter lengths) of the transistor are chosen either to fulfill an impedance matching [1], [4] or to enforce a constant power limitation [2], [3].

In all these referred papers, LNAs were built considering a narrowband frequency operation for a particular wireless standard. As the communication technology advances, however, different standards have appeared each of which requiring a specific receiver structure. In order to establish communication systems capable of operating over a frequency band,

RF building block designs should be changed such that they exhibit their narrowband properties at several distinct frequencies. Thus, LNAs need to be modified as well, such that they maintain their NF and high gain characteristics for the whole frequency range. In that respect, reconfigurable circuit blocks pose a solution method. By incorporating tunable reactive components to the LNA topology, the noise figure and input/output matching results in the narrowband can be accomplished at other frequencies.

In this paper, a novel topology and an algorithmic design procedure for tunable LNAs based on HBTs are proposed. The suggested topology eliminates the series inductor at the base of the HBT device and replaces it with a π -matching network. This allows the designer sufficient flexibility to choose the on-chip reactive component values in the matching network. Besides, if the series capacitors at the input and output matching networks are made tunable, the outstanding properties of the LNA at narrowband operation can be translated to neighboring frequencies.

2. The Derivation and Demonstration of the Design Procedure

2.1. Principles of Low Noise Design

To guarantee the operation with the minimum noise figure and maximum possible gain, the input impedance and optimum noise impedance presented by the core LNA should match with the source impedance. This condition can be decomposed into its real and imaginary parts as given in (1) and (2).

$$R_S = R_{IN} = R_{S,OPT} = R_{OPT} \quad (1)$$

$$X_S = X_{S,OPT} = -X_{IN} = -X_{OPT} \quad (2)$$

The procedure has been developed using SiGe HBTs. The bipolar transistors can be best analyzed for their noise characteristics by means of their small

signal model. In this case, a hybrid- π model has been utilized. The shot noise sources originating from the base-collector and base-emitter junctions as well as the thermal noise source at the base of the HBT have been considered. By modeling the HBT as a two-port network, transfer functions relating the input and output ports have been derived with which the contributions of each noise source to the input referred noise have been quantified. At the end of this process, the input equivalent voltage and current noise sources, $\langle v_{IN} \rangle^2$ and $\langle i_{IN} \rangle^2$ respectively are acquired. These two quantities describe fully the input referred noise content which is the critical information for low noise design. In the next step, using $\langle v_{IN} \rangle^2$ and $\langle i_{IN} \rangle^2$, the chain correlation matrix C_A given in (3) will be developed. The correlation between $\langle v_{IN} \rangle^2$ and $\langle i_{IN} \rangle^2$ is anticipated since the same noise sources are contributing to both of these quantities. Also, R_{OPT} and X_{OPT} can be expressed using the correlation matrix C_A via the well-known formulas (4) and (5) [5].

$$C_A = \frac{1}{4k_B T \Delta f} \begin{bmatrix} \overline{v_{in}^2} & \overline{v_{in} i_{in}^*} \\ \overline{i_{in} v_{in}^*} & \overline{i_{in}^2} \end{bmatrix} = \begin{bmatrix} C_{A,11} & C_{A,12} \\ C_{A,21} & C_{A,22} \end{bmatrix} \quad (3)$$

$$\frac{1}{R_{OPT}} = G_{S,OPT} = \sqrt{\frac{C_{A,22}}{C_{A,11}} - \left[\frac{\text{Im}(C_{A,12})}{C_{A,11}} \right]^2} \quad (4)$$

$$-\frac{1}{X_{OPT}} = B_{S,OPT} = \frac{\text{Im}(C_{A,12})}{C_{A,11}} \quad (5)$$

The elements of C_A have been rigorously derived for bipolar transistors assuming ideal passive elements so that relatively complex expressions have been acquired which are simplified based on practical assumptions [6]. Here, the results reached using these approximate terms will be presented and discussed.

2.2. Theoretical Derivation of the Procedure

Figure 1 depicts the topology on which the design procedure will be applied. Like in other LNA structures, an emitter inductor L_e is utilized to improve linearity and to satisfy the low noise design constraint $R_{IN}=R_{OPT}$ along with C_{ex} across C_π . A high-pass L-type matching structure is combined with the bias inductor L_c , so that a π -matching network can be built. L_c makes sure that the other low noise design condition $X_{IN}=X_{OPT}$ can be met. Afterwards, with the help of $C_{m,in}$ and $L_{m,in}$, these reactances are resonated out whereas the whole π -network matches the equalized R_{IN} and R_{OPT} to R_S . The cascode structure has been

chosen for the amplifier to boost the isolation between the input and the output matching network which is built using a high-pass L-type matching structure. The biasing network supplies the necessary voltages to the bases of Q_1 and Q_2 .

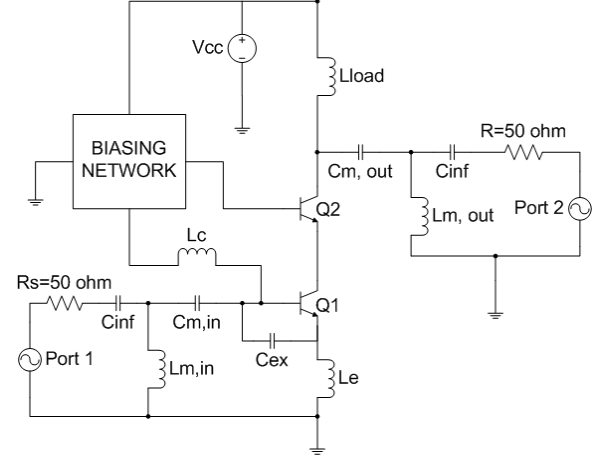


Figure 1. The proposed design topology

The design procedure focuses on the common-emitter transistor Q_1 since the total input referred noise is mainly determined by this device. As the first step of the proposed methodology, the optimum current density $J_{C,OPT}$ that will result in the NF_{MIN} operation is determined. So, the biasing network should be built such that the DC voltage that will establish $J_{C,OPT}$ is applied to the base of Q_1 . Subsequently, the input resistance R_{IN} looking at the base of Q_1 into the device should be brought to the same value with the optimum noise resistance R_{OPT} evaluated at the same place. For this purpose L_e and C_{ex} need to be determined carefully. By returning to the correlation matrix C_A , an approximate design equation revealing the relationship between L_e and C_{ex} can be developed. The simplified expressions for $C_{A,11}$, $C_{A,22}$, $\text{Im}(C_{A,12})$ and R_{OPT} – disregarding L_c and including it in the remaining matching structure- can be acquired by combining C_π and C_{ex} under the term C_{be} , as given in (6)-(9):

$$C_{A,11} \approx r_b + \frac{[1 - 2\omega^2 L_e C_{be}]}{2g_m} \quad (6)$$

$$C_{A,22} \approx \frac{\omega^2 (C_{be} + C_\mu)^2}{2g_m} \quad (7)$$

$$\text{Im}(C_{A,12}) \approx -\frac{[\omega (C_{be} + C_\mu)](1 - \omega^2 C_{be} L_e)}{2g_m} \quad (8)$$

$$R_{OPT} = \frac{1}{G_{S,OPT}} \approx \frac{\left[1 + 2(g_m r_b - \omega^2 L_e C_{be})\right]}{\omega \sqrt{2g_m r_b (C_{be} + C_\mu)}} \quad (9)$$

After determining R_{OPT} , R_{IN} could be found by calculating the input equivalent resistance of the LNA.

$$R_{IN} \approx \frac{r_\pi + \omega^2 r_\pi^2 L_e C_{be} g_m}{\omega^2 r_\pi^2 C_{be}} \approx \frac{g_m}{C_{be}} L_e \quad (10)$$

By setting (9) and (10) equal, a design equation for the emitter inductor L_e can be developed as shown in (11):

$$L_e \approx \frac{2g_m r_b + 1}{\omega \left(g_m \sqrt{2g_m r_b + 2\omega C_{be}} \right)} \quad (11)$$

Equation (11) confirms the expectations that the extra base-emitter capacitor actually lowers the necessary value for L_e to realize the equality between R_{IN} and R_{OPT} .

In the next step, the reactive parts of Z_{IN} and Z_{OPT} should be reconciled. For this purpose, the bias inductor L_c will be used extensively. A similar theoretical analysis can be conducted in order to verify the importance of L_c in this process. Firstly, X_{OPT} will be calculated by incorporating L_c in the noise analysis. So, the π -network will be decomposed and the remaining components, $L_{m,in}$ and $C_{m,in}$, are going to be used to resonate out the equalized reactance at the base of Q_1 .

$$\text{Im}(C_{A,12}) \approx \frac{\left[\omega L_e g_m^2 \left(\frac{L_e}{L_c} \right) + \frac{1}{\omega L_c} \right]}{2g_m} = \frac{1 + \omega^2 L_e^2 g_m^2}{2\omega L_c g_m} \quad (12)$$

Equation (12) has been derived by considering the transfer functions between the input and output port while looking into the core LNA. Thus, it contains the negativity which is indicated in (5). Based on this fact, the negative sign in (5) will be dropped and the expression for X_{OPT} is reformulated as follows:

$$X_{OPT} \approx j \frac{r_b + \left[\frac{1 + (\omega L_e g_m)^2}{2g_m} \right]}{1 + \omega^2 L_e^2 g_m^2} \approx j\omega L_c \quad (14)$$

Next, X_{IN} will be evaluated in a way similar to R_{IN} . It is to observe that both (14) and (15) depend on L_c heavily.

$$X_{IN} \approx j \left[\omega L_c \parallel \left(\omega L_e - \frac{1}{\omega C_{be}} \right) \right] \approx j\omega L_c \quad (15)$$

L_c is in parallel with the reactance of the core LNA. It should present a small impedance in order to dominate in (15) as desired. It is also noteworthy to realize that with the proper selection of L_c , X_{IN} and X_{OPT} can be brought to the same level without further design complications.

At the last step, $C_{m,in}$ and $L_{m,in}$ should be assigned values to resonate out the reactance present at the base of Q_1 and match R_{IN} and R_{OPT} to the port resistance R_S as a π -network with the inclusion of L_c . This can be managed by using the classical equations of matching networks.

2.3. Demonstration of the Procedure

The design procedure has been demonstrated by constructing a LNA operating at 5 GHz using the IBM 0.18 μm (7HP) design kit. All inductors are built as spiral inductors. Even though the equations are developed by assuming ideal passive elements, they yield approximate values for the design quantities and by the help of the simulation tools, exact results can be reached after a short manipulation process. $J_{C,OPT}$ has been acquired for a potential of 0.83V applied to the base of Q_1 . Q_2 is biased with 1.4V at its base. The emitter lengths are chosen to be 19.2 μm and L_{load} is assigned to be 1.05 nH. Moreover, by selecting L_c 326 pH and C_{ex} 220 fF, R_{IN} and R_{OPT} can be made equal as shown in Figure 2.

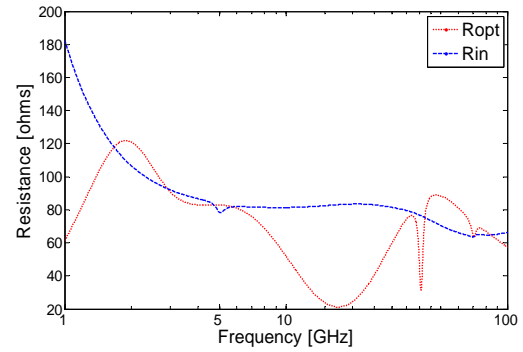


Figure 2. R_{OPT} and R_{IN} vs. Frequency

In a similar manner the reactances are brought to the same value with the bias inductor L_c of 1.03 nH. X_{IN} and X_{OPT} for the finalized design can be visualized in Figure 3. The slight differences between the quantities at 5 GHz which can be observed in Figure 2 and Figure 3 are negligible.

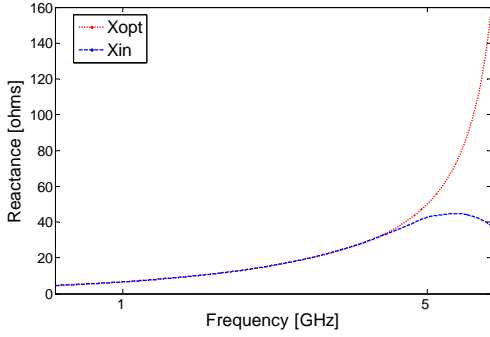


Figure 3. X_{OPT} and X_{IN} vs. Frequency

Then, the matching networks are established using the resistive and reactive components of Z_{IN} and Z_{OPT} . By using the matching network equations and simulation process, $L_{m,in}$ and $C_{m,in}$ are found to be 1.23 nH and 490 fF, respectively. The output matching network is composed of $L_{m,out}=350$ pH and $C_{m,out}=730$ fF. As can be realized from the values of matching network elements, all of them are below 1.25 nH and they can be built as integrated components. Moreover, $C_{m,in}$ is in series at the base of the HBT and it will be demonstrated that with the help of $C_{m,in}$, the LNA can be made tunable.

In Figure 4, the NF performance of the designed LNA can be seen. At 5 GHz, NF of the LNA is about 2.18 dB whereas NF_{MIN} can be read as 2.16 dB. These values confirm that the noise matching is achieved.

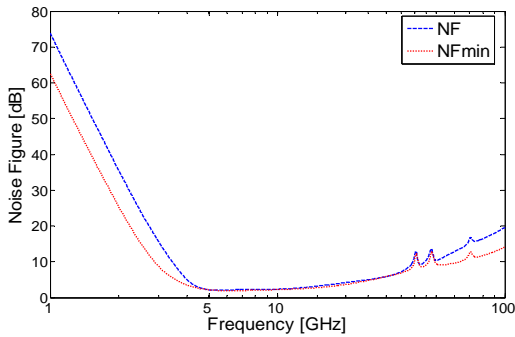


Figure 4. NF and NF_{MIN} vs. Frequency

Similar results are to observe in Figure 5. Here, the input return ratio (S_{11}) is -34.2 dB with a transducer gain (S_{21}) of 16.8 dB. The output return ratio can be found as -15.2 dB. These results indicate that the input power match has succeeded as well. Finally, even though the linearity constraints of LNAs are not imposed on the design procedure, IIP3 simulations

have been conducted where IIP3 is found to be -7 dBm, which is acceptable.

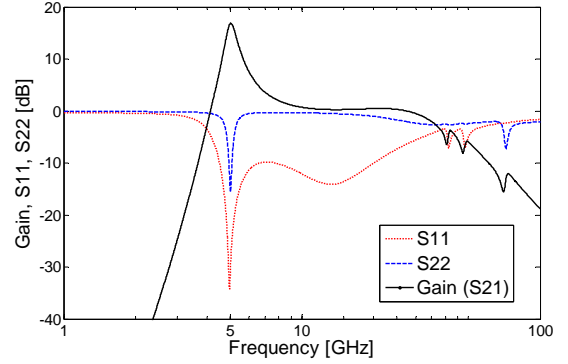


Figure 5. S_{11} , S_{22} , and Gain (S_{21}) of the LNA vs. Frequency

3. Tunability Analysis

As the second part of the strategy, the tunability options are considered for the designed LNA. Exact behavior of the circuit could be translated to other frequencies by changing the values of all reactive components used in the design procedure. However, due to the low performance of on-chip tunable components, this option cannot be applied. In this work, it is preferred to assume only the reactive components tunable that yield the biggest frequency range for which the acquired results at narrowband can be preserved. In that respect, series matching capacitors $C_{m,in}$ and $C_{m,out}$ are chosen. It should be noted that a tunable capacitor is easier to fabricate than a variable inductor.

The series input matching capacitor $C_{m,in}$ can be thought as a combination of two series capacitors having the values $C_{m,1}$ and $C_{m,2}$, depicted in Figure 6. To cancel out all reactances in the matching network, the impedance of $C_{m,2}$, $X_{Cm,2}$, should be equal to X_{Lc} .

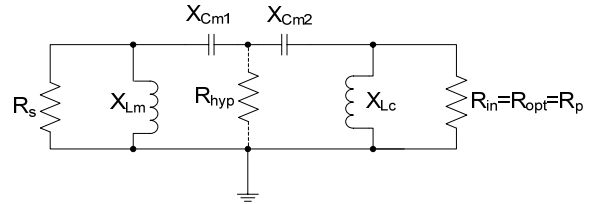


Figure 6. Decomposed π -matching network

Similarly, $X_{Cm,1}$ has to compensate for X_{Lm} . Here, it has been assumed that the resistance values of R_s and R_p are much higher than the inductor impedances of L_m and L_c , respectively. Finally, the hypothetical

resistance R_{hyp} is used to satisfy the real impedance matching of R_{OPT} and R_{IN} to R_S .

In the last step, for a number of different frequencies around the center frequency (5 GHz) the required values of $C_{m,in}$ and $C_{m,out}$ are recorded through simulations while they are modeled as normal capacitors from the design kit. Figure 7-9 show if the values of $C_{m,in}$ and $C_{m,out}$ are appropriately chosen, for the range of 3.5-6.5 GHz, S_{11} and S_{22} values are found to be below -10 dB and the difference between NF and NF_{MIN} to be less than 0.5 dB. A feasibility analysis indicates that the capacitance values presented in Figure 9 can be realized in the near future considering the rapid development in the tunable capacitor technologies [6]. Thus, next steps should be specifying the operation parameters of the tunable capacitor such as the quality factor and the self-resonance frequency. It should also be inquired how the variations in the values of these parameters change the operation characteristics of the tunable LNA.

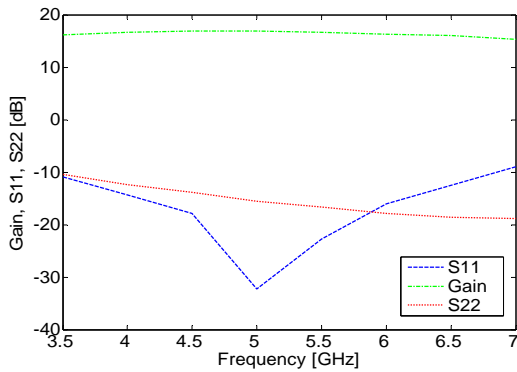


Figure 7. The gain, S_{11} and S_{22} performance of the tunable LNA

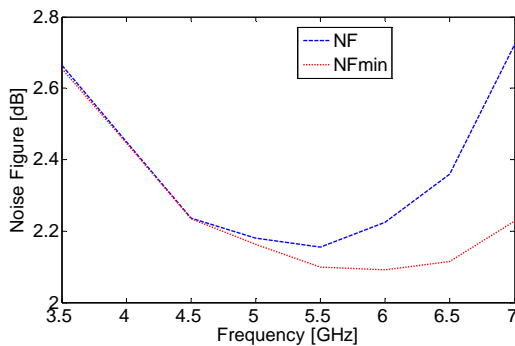


Figure 8. The NF and NF_{MIN} performance of the tunable LNA

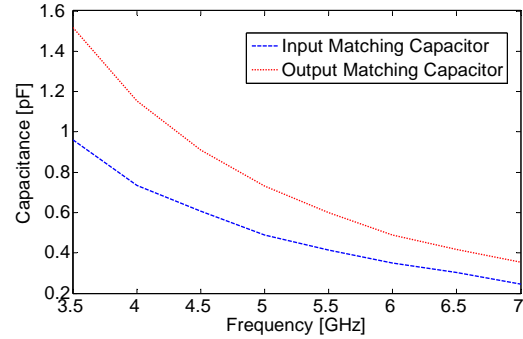


Figure 9. Necessary capacitance values for the tunable LNA

4. Conclusion

A novel design procedure has been developed from theoretical relations and is shown via an example design. The methodology is based on a different matching strategy compared to its counterparts and does not rely on any unchangeable quantities during the operation such as the emitter length. Additionally, it enables the designer to build tunable LNAs in frequency domain by varying the single series capacitor in the input/output matching networks.

5. References

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