

A 90nm CMOS Direct Conversion Transmitter for WCDMA

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Abstract — A linear high output power CMOS direct conversion transmitter for wide band code division multiple access (WCDMA) is presented. Circuit level third order distortion cancellation is applied to driver amplifier to achieve single end output power +9.6 dBm with -43.2dBc ACLR@5MHz and 10% power efficiency at band II. The transmitter is fabricated in 90nm CMOS technology and die area is 1.1mm × 1.4mm. The transmitter consumes 91.4mW while delivering +9.6 dBm output power. The VDD supply for upconverter is 1.4V, and the VDD for driver amplifier is 3V. The packaged type is 32 pins 5×5 QFN.

Index Terms — direct conversion, CMOS, WCDMA, transmitter, third order distortion cancellation, linearity, power efficiency.

I. INTRODUCTION

In modern mobile communications, the need for the low cost, low power and small form factor is tremendous. One method of achieving this target is through high level integration by eliminating costly external components. Direct conversion transmitter draws more and more attention due to its inherent compactness and ease for integration than heterodyne architecture. CMOS technology is amenable to high level integration due to the fact that vast majority of digital integrated circuits are developed by this technology. Hence, a direct conversion CMOS transmitter is very attractive for reducing chip area and cost considerably.

For WCDMA system, one of design challenge is to design a linear transmitter. As opposed to GSM system, the nonconstant envelope modulation requires linear amplification to guarantee modulation accuracy. There are two specifications [1] related to linearity requirement of user equipment for frequency division duplex (FDD) mode universal mobile telecommunications system (UMTS). One is the error vector magnitude (EVM), which has to be 17.5% below for WCDMA system; the other is adjacent channel leakage ratio (ACLR), which is specified to be -33dBc. EVM can be defined in term of SNR, and 17.5% EVM is corresponds to SNR 15.1dB. So, in term of linearity specification, -33dBc ACLR is more stringent than EVM 17.5%. Moreover, considering most nonlinearity coming from power amplifier, the target linearity of transmitter is desirable to be 10dB back off

from the UMTS user equipment specification to allow power amplifier to dominate the linearity budget. The target output power for this design is 10dBm. Section II shows power budget of the transmitter chain to explain why the 10dBm output power is desirable. Considering the driver amplifier to be a class AB amplifier for achieving reasonable power efficiency, it is a big challenging to design a linear CMOS transmitter that meet -43dBc ACLR@5MHz at 10dBm output power.

Comparing recently published direct conversion transmitter/transceivers for WCDMA designed in CMOS technology [2, 3] or SiGe BiCMOS technology [4-6], it shows that it is more challenging to implement a linear transmitter in CMOS technology. As shown, the transmitter in [2] reported -38dBc ACLR@5MHz at 2.5dBm output power and that in [3] reported -38dBc ACLR@1.92MHz at 6dBm output, while the design using SiGe BiCMOS [5] shown that output power 9.5dBm with -46dBc ACLR@5MHz. However, as modern wireless communications system calls for transition from SiGe BiCMOS to CMOS technology, and employs even higher data rate modulation schemes, there is an increasing demand for linear CMOS transmitter in recent years. This paper presents a linear high output power CMOS 90nm direct conversion transmitter for WCDMA systems with good power efficiency.

This paper is organized as follows. Section II outlines the architecture of the direct conversion transmitter. Section III describes circuit building blocks including upconverter and driver amplifier. Section IV shows the measurement results, and section V concludes papers.

II. DIRECT CONVERSION TRANSMITTER ARCHITECTURE

Fig. 1 shows a block diagram of the direct conversion WCDMA transmitter chain illustrating the signal path from baseband all the way up to the RF output at the antenna. I and Q signal coming out of based band filter are feed into I and Q upconverter respectively, then the modulated signals are combined together before passing through driver amplifier. A surface acoustic wave (SAW) filter is placed between the PA and driver amplifier to remove out of band noise, which falls within the receiver

band. Because WCDMA system need about 90dB gain control range, usually the driver amplifier also implements gain control to serve as a radio frequency variable gain amplifier (RFVGA). This design focuses on the linearity/power efficiency rather than gain control, hence, no gain control is implemented in this version of the design, and the gain control will be implemented in the next version. The upconverter output stage adopted in the design is a cascode stage amplifier, which will be designed to serve as step gain control amplifier in the next version. This paper describes the design of TXIC part shown in block diagram Fig. 1, which includes I/Q upconverter, driver amplifier and quadrature divider.

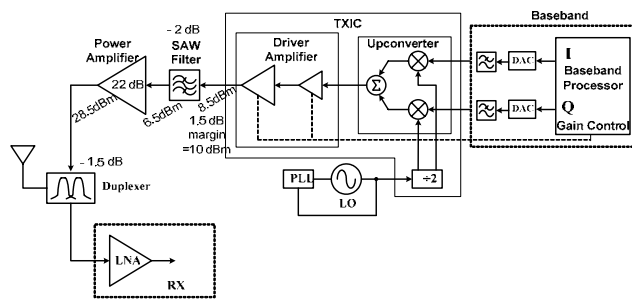


Fig. 1. Block diagram of a direct conversion transmitter.

The target class of WCDMA operation for this transmitter is class 2 which specifies an output power of 27dBm +1dB/-3dB. Typical insertion loss of duplexer of transceiver is 1.5dB, so the output power of the power amplifier should be at the range of 28.5dBm. To keep the gain of PA down to a level that a two stage amplifier can easily support, assume the gain of two stages PA is 22 dB and the insertion loss of SAW filter is 2dB, the output of transmitter should be 8.5dBm. Considering 1.5 dB margin for gain variation in the PA and duplexer, a 10dBm output power of transmitter is desirable.

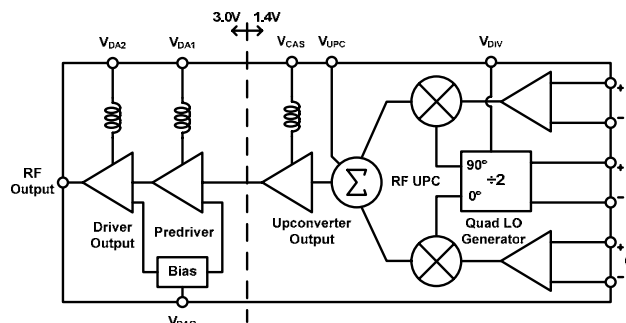


Fig. 2. Block diagram of the implemented TXIC.

III. CIRCUIT DESIGN

Fig. 2 shows a block diagram of input, output, and power supply of the TXIC implemented in the design. Dual oxide transistors are available for the 90nm CMOS technology used in this project. To take the advantage of thin oxide of 90nm transistor, upconverter is designed by using thin oxide transistor, while the driver amplifier is designed with thick oxide devices. As shown, the power supply domain is divided into two areas where the driver amplifier, predriver, and their bias circuits are operated at 3V while the upconverter and quadrature LO generator circuits are operated at 1.4V supply voltage due to the use of thin oxide 90nm devices.

Design reliability is considered in the design. It is well known, gm degradation in MOSFET device occurs due to the hot carrier injection effect. Hence, instead of minimum channel length, 0.2um is used for thin oxide transistor and 0.4um is used for thick oxide devices.

A. Upconverter

Fig. 3 shows schematic of the quadrature I and Q upconverter. The core of the upconverter is double balanced mixer for both I & Q channel. However, there are modifications compared to a traditional Gilbert cell double balance mixer. First, folded differential pair is adopted for the input transconductor. Folded input pair helps to alleviate the headroom crunch and allows the input common mode voltage to be flexible. Second, current mirror load is used for differential to single-ended conversion. Compared to using an on chip balun, this saved board space and has less loss. Third, for the folded differential input pair, a CMOS version multi-tanh triplet [7] is used to improve the linearity of input differential pair.

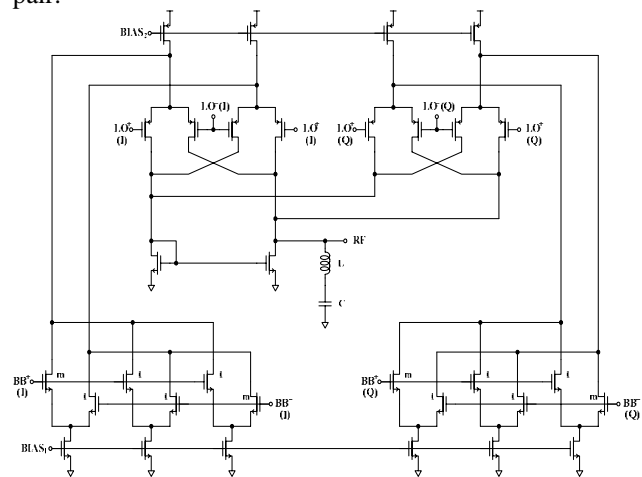


Fig. 3. Simplified schematic of upconverter,

The output stage of upconverter is a cascode amplifier which provides good isolation between upconverter and driver amplifier. The need for isolation is because both two stages of driver amplifier are common source amplifiers, in which case the impedances of the tuned LC resonance circuits are sensitive to the output impedance of the upconverter. If the impedances are changed, then the characteristic of the driver amplifier is changed due to gain and phase variation. The second reason is that cascode amplifier stage gives additional voltage gain for delivering a 10dBm output. Another benefit is that RF gain control can be more easily implemented at this cascode amplifier without impairing the third order distortion cancellation of driver amplifier.

B. Driver amplifier

Fig. 4 shows the schematic of upconverter output stage and driver amplifier. The driver amplifier is composed of two stages. Both two stages of driver amplifier are class AB amplifier. The voltage gain of the final stage is about 6 dB. To deliver a 10dBm output power, the input amplitude of the final stage has to be large; hence, the final stage of driver amplifier is a nonlinear large signal class AB amplifier. Assume a two tone signal is applied into the final stage; the third-order distortion will generate $2f_1-f_2$ and $2f_2-f_1$ components, which is not desirable because it will fall within the adjacent channel. Usually linearity comes at the price of the low power efficiency. To mitigate this trade off between the linearity and power efficiency, third order distortion cancellation is applied to driver amplifier. The basic idea is that the third-order distortion generated by the prestage of driver amplifier is used to cancel the third-order distortion generated by the final stage of the driver amplifier.

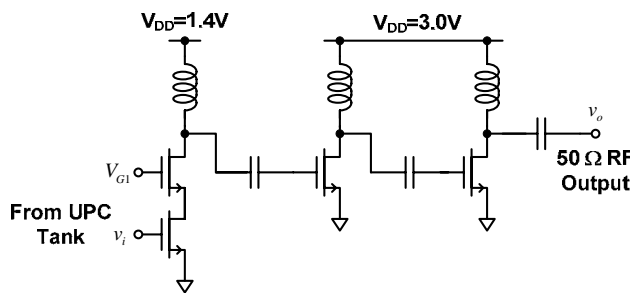


Fig. 4. Schematic of upconverter output stage and two stages driver amplifier.

The cancellation of the third-order distortion can be represented by Fig. 5, where block P represents the prestage of driver amplifier and block F represents final stage of driver amplifier. P1, P3, F1, F3 correspond to first-order, third-order transfer function respectively. The

third-order components are generated by both F3 and P3 blocks. F3 generates third-order components from the fundamental components that coming out from P1 blocks. Also, the third-order components generated by the block P3 and amplified by block F1 shows as a part of final output distortion. If the third order distortion generated by P3 and amplified by block F1 is of same magnitude and 180 phase degree difference than that generated by the F3 blocks, the output third order distortion of final stage will decrease dramatically. Fig. 6 envelope simulation result shows that the third order distortion of driver amplifier's final output is much small than that of input of final stage due to the third order distortion cancellation. One thing worth to be mentioned here is that third order distortion will also be generated due to the mixing of second-order harmonic or envelop components with fundamental components. Because they are small compared to the third order distortions generated by F3 and P3, to simplify the illustration of third order cancellation, it is omitted here.

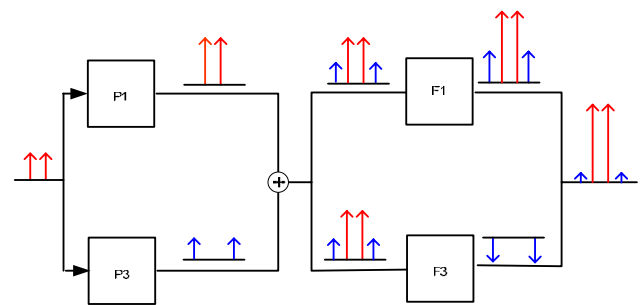


Fig. 5. Simple representation of third order distortion of a two-stage amplifier.

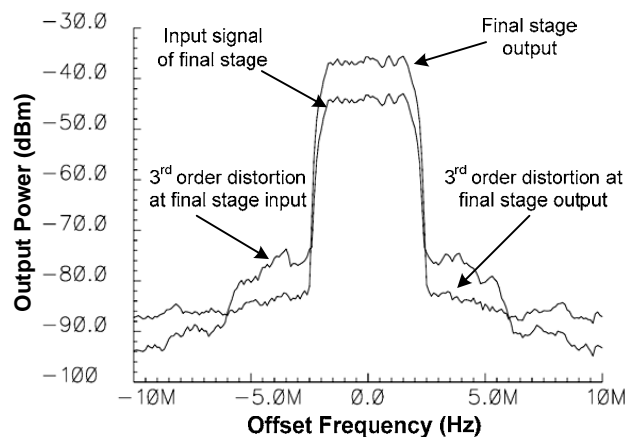


Fig. 6. Simulated spectral of input and output of final stage of driver amplifier.

IV. MEASUREMENT

The transmitter frequency response was measured by sweeping the LO input frequency from 1.45 GHz to 2.0 GHz while the baseband inputs were driven by a modulated WCDMA uplink signal. The measured output power and ACLR results are displayed in Fig. 7. Clearly the center frequency is around 1.7 GHz which is 12.8% lower than 1.95 GHz. There are two explanations for this deviation. First, in order to achieve good third order distortion cancellation, the center frequency of driver amplifier's LC tank is intentionally designed to be less than 1.95GHz. However, because the center frequency of the upconverter output stage is designed at 1.95GHz, the output power at 1.7GHz is suppose to be about the same as 1.95GHz. The second reason may be due to deviation of foundry library inductor models which also yielded similar tuning errors in other designs employing the same model. Fig. 8 shows the power efficiency of the transmitter and that of two stages driver amplifier. As shown, the power efficiency of two stage driver amplifier can achieve 15.2% at +10.4dBm with -41.3dBc ACLR@5MHz at 1.85GHz, which is a typical value for linear CMOS power amplifier, however, power amplifier delivers much higher output power.

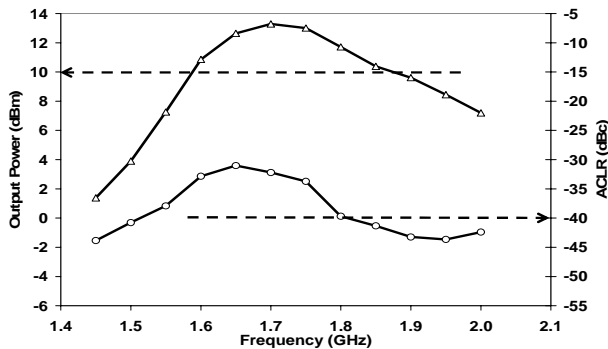


Fig. 7. Measured output power and ACLR versus LO frequency.

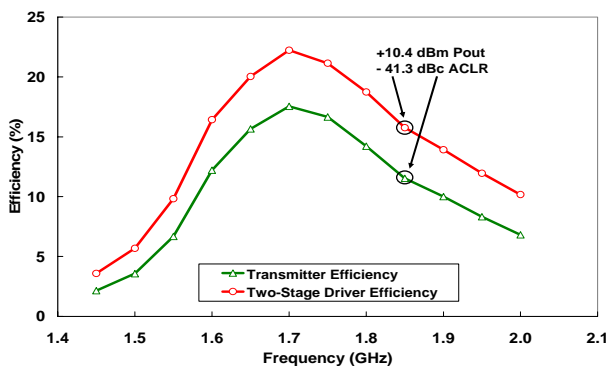


Fig. 8. Measured power efficiency versus LO frequency.

V. CONCLUSION

A linear high output power 90nm CMOS direct conversion transmitter for WCDMA system is presented. In order to mitigate the trade off between power efficiency and linearity, circuit level predistortion technology is applied to driver amplifier. The transmitter achieved +9.6 dBm single end output power with -43.2dBc ACLR@5MHz and 10% efficiency at 1.9 GHz. The result shows a CMOS transmitter with exceptional linearity performance and power efficiency which indicate CMOS transmitter can achieve potential competition to the published BiCMOS transmitter.

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