

Integrated Time Division Multiplexing Front-End Circuit for Multi-Antenna RF Receivers

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Abstract — A fully integrated receiver front-end circuit for a 4:1 time division multiplexing of RF signals from an antenna array is introduced. The switching necessary for multiplexing is implemented as an array of low noise amplifiers operating at 2.4 GHz with selectable outputs. The circuit includes on-chip input and output matching networks. A digital controller for rotating through the amplifier inputs was also incorporated. The multiplexer design was fabricated in a 0.18 μm RF-CMOS process. Measurement and post processing results are presented to demonstrate that such a RF multiplexing system can properly recover signal relative phase/amplitude variations at the individual inputs of a multi-antenna receiver. Such a front-end is useful for a variety of antenna array communications applications.

Index Terms — Time division multiplexing, array signal processing, diversity methods, switching circuits, amplifiers.

I. INTRODUCTION

Antenna diversity, beamforming and MIMO techniques are emerging as increasingly attractive options in integrated wireless receivers because of the numerous advantages they offer [1]. Two characteristics common to all these methods are multiple antenna receiver architectures and incorporation of more digital signal processing closer to the antenna. The performance benefits of multi-antenna receivers include increased channel capacity for MIMO and diversity systems and directional gain in beam steering arrays. However, the benefits of these systems are partially offset by increased cost and power consumption of simultaneously operating multiple receivers.

To date, commercial integrated MIMO and diversity systems have relied on brute force replication of receiver chains to provide improvements in capacity. This approach, as expected, entails an excessive power, silicon area and cost penalty. Time division multiplexing multiple RF inputs into one signal path is an attractive approach for reducing the power consumption and hardware complexity of multiple antenna receiver architectures. The concept of periodic antenna switching to combine multiple RF signals into a single receive channel has been around for a while [2, 3]. A similar concept was used in the front-end design of a 3:1 multiplexer [4] for a HP network/spectrum analyzer to enable two-port vector measurements using a

single receiver. Recently the Spatial Multiplexing of Local Elements (SMILE) was introduced as a time division multiplexed scheme for digital beamforming [5, 6] which achieves a reduction of RF hardware by multiplexing several individual elements of the antenna array into a single RF channel prior to the downconversion mixer. The switching is performed at a high enough rate for the desired signal attributes at each antenna to be recoverable at baseband.

This paper presents a new integrated time division multiplexed RF front-end design where the RF multiplexing function occurs just after signal amplification to simplify integration, provide good channel isolation, and provide the capability of maintaining a constant impedance match on each antenna port at the expense of a small increase in power consumption. A 4:1 multiplexer design for a 2.4 GHz front end implemented in a 0.18 μm CMOS process is presented. Digital oscilloscope measurements of the output multiplexed RF signal in conjunction with signal post processing demonstrate accurate symbol recovery from each RF channel.

II. SYSTEM ARCHITECTURE

The system block architecture for spatial time multiplexed RF receiver is shown in Fig. 1. The general function of frequency downconversion retains the form of conventional receiver architectures such as superheterodyne, direct conversion, or low IF. The most important changes are in the receiver front-end design and baseband processing. In the front-end, RF signals from an N element antenna array are serialized into a single RF signal path. At baseband the signals are split into separate antenna data streams by demultiplexing. All sampling and switching (including multiplexing) operations right from the front-end onwards are under synchronous clock control. The hardware area and power consumption savings of this multiple antenna receiver architecture are appreciable even when considering the increased baseband processing requirements.

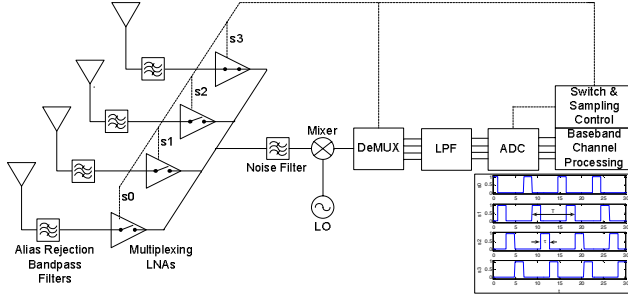


Fig. 1. Time Division Multiplexing receiver architecture (Inset: Switch control pulses).

The fundamental sampling requirement for recovering data from each of the antenna elements is given by the well known Nyquist sampling theorem. Assuming a real-valued bandpass signal of bandwidth B centered at carrier frequency f_c , to avoid spectral aliasing each element of the array must be sampled at a rate:

$$f_s \geq 2B. \quad (1)$$

Bandpass sampling however does not permit f_s to be arbitrarily chosen as any value satisfying condition (1) as this could lead to overlapping of aliases that could corrupt the information signal depending on its band position. f_s may be optimally chosen as:

$$f_s = \frac{4}{2p+1} f_c \quad (2)$$

where p is an integer. This centers the signal spectrum and its aliases in the Nyquist sampling zones, thus simplifying alias rejection filtering and downconversion. In an N element array, the net sample rate for all channels being multiplexed into a single RF stream, termed the multiplexing rate is:

$$f_{max} = Nf_s \quad (3)$$

In the frequency domain, replication of the signal spectrum forming the actual information bandwidth would be evident due to the sampled nature of the signals in time, the sampling being done with rectangular pulses. The spectral components repeat at intervals of f_s in the frequency domain and their envelope has the characteristic $sinc(x)$ shape. This is seen in both the multiplexed signal, which is the sum of pulsed RF antenna signals, as well as in the demultiplexed signal at baseband. At baseband the signals are demultiplexed in analog domain into separate antenna channels for further processing. After being digitized into multiple antenna data streams, enhanced information channel processing may be completed digitally to derive whatever advantages that the antenna array system has to offer.

III. CIRCUIT DESIGNS

A. RF Switching Amplifiers

The multiplexing front-end is formed by a parallel arrangement of identical low noise amplifier (LNA) switch cores with a single output matching network. High isolation between inputs and output is required for the LNAs to be able to function satisfactorily without affecting each others performance. The cascode LNAs are designed with current switching action intrinsic to their topology. Therefore, another requirement for this architecture is to ensure that the switching speed is not affected due to their parallel connection. The circuit implementation of the multiplexing front-end of Fig. 1 is as shown in Fig. 2.

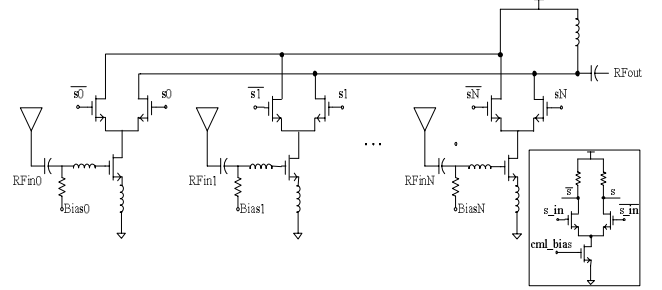


Fig. 2. Circuit implementation of Multiplexing LNA (Inset: Switch drive buffer).

Each LNA core receives a differential control signal from a switch drive buffer. The LNA core itself is designed around the single-ended cascode topology. The cascode amplifier topology provides high input-output isolation while maintaining a sufficiently low noise figure and adequate gain. The switching is incorporated into the cascode architecture easily by switching the cascode device between cutoff and saturation using a current steering differential pair switch, with one switch being diverted to the supply. The differential switching action also ensures that the each antenna element sees an almost constant input matching regardless of whether the associated channel is 'on' or 'off'. This assists with maintaining a uniform feed network loading as the 'on' switch position rotates through the switch array.

The inputs and output were matched to 50Ω with on-chip matching networks comprised of parallel stacked spiral inductors and dual MIM capacitors. The input and output matching were offset from each other for a flatter gain response over a wider bandwidth. Each LNA core had its own current mirror device for biasing.

Current Mode Logic (CML) buffers of the type shown in Fig. 2 were used to drive the LNA switches in order to reduce signal swings to $\sim V_{DD}/3$ at the switch device gates and lower the control signal feedthrough to the RF output.

The current consumption per CML buffer was 2 mA. The differential buffers are controlled by the outputs from a digital controller section.

B. Digital Controller

The controller was designed for high speed operation. The Hybrid Latch Flip Flop (HLFF) was used in the digital circuits for the superior performance it offers without a large power penalty. The controller itself had to cycle through each of the LNA switches in turn at rates governed by relation (3). The ring counter topology seen in Fig. 3 was used to obtain a one-hot controller output.

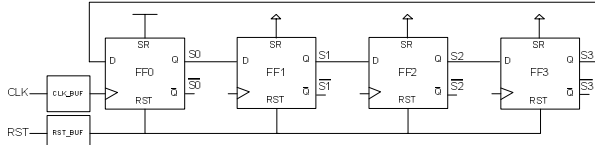


Fig. 3. Digital controller for RF multiplexing

In order to limit the number of control inputs to the circuit to simplify testing, only two digital inputs were provided for: clock and reset. A direct-drive Chappell receiver was used in the clock buffer to permit direct interfacing to a 50 Ω pulse generator. Simulations with parasitics extracted indicated that the controller was able to operate correctly for rates well over 1 GHz.

IV. MEASUREMENT RESULTS

The circuit was realized in 0.18 μm RF-CMOS technology. The circuit die photograph is shown in Fig. 4. ESD protection was provided for on all pads. Testing was done on-wafer by probing. Each LNA was biased ~ 5 mA of current from a 1.8 V supply and the CML buffer biased to develop 600mV of swing below V_{DD} .

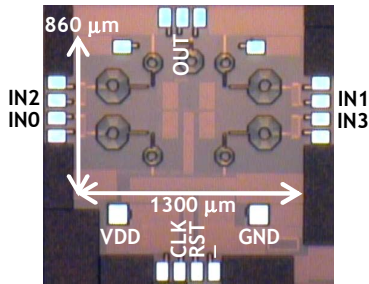


Fig. 4: Circuit die photograph of 0.18 μm CMOS design.

A. Amplifier Response: S -parameter Measurements

The measured S_{11} and S_{21} between Port 1 = RFin1 and Port 2 = RFout are shown in Fig. 5 as the controller cycles through each of the LNAs in turn. The shown response was typical of other channels too. The power gain was 2.6 dB at 2.4 GHz and produced gain over a wide bandwidth

of 1.77 GHz around this center frequency. Although the static gain is useful if the LNA is used in its conventional sense, in a multiplexed context a more relevant gain would be the dynamic or conversion gain for the 0th harmonic. This power gain would be below the static gain by a factor of $20\log N$ (12 dB here). This fact was confirmed by comparing input and output signal spectra. LNA on-off isolation was observed to be in the 16-20 dB range. The poor output matching S_{22} of -3.2 dB contributed to the lower gain of the amplifier. The disturbance in matching was identified to be primarily due to unaccounted parasitic resistances in the circuit layout. However, the lower gain did not prevent the testing of the RF multiplexing idea proposed in this work.

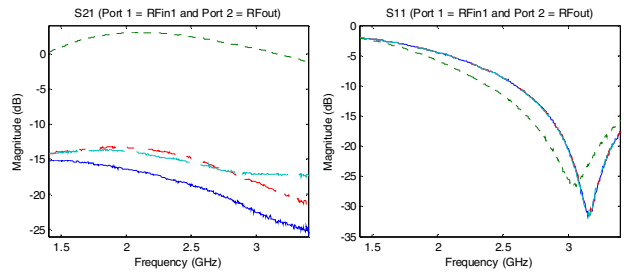


Fig. 5. LNA S_{11} and S_{21} with Port1=RFin1 and Port2=RFout [— : Ch0_On, -- : Ch1_On, ···· : Ch2_On, - - - : Ch3_On].

B. Multiplex Operation: Time Domain Processing

In order to gauge the usefulness of the circuit as a front-end for multi-antenna systems leveraging beamforming or diversity advantages, the test setup had to include ways of introducing known phase/amplitude relationships at the different RF inputs. To that effect, the RF inputs were supplied from a single signal source producing a Gray Coded QPSK modulated RF signal split into multiple paths for the multiple inputs, with independently controllable phase shifters on each path. The controller was given a free running clock from a pulse generator. The RF output from the circuit went to a vector spectrum analyzer whose 70 MHz IF output was then connected to a real time digital oscilloscope. The VSA IF bandwidth was restricted to 40 MHz, hence a multiplex rate f_{max} of 20 MHz was chosen. The per channel pulse rate f_s was thus 5 MHz. A symbol rate of 1MSymb/s with Root Nyquist filtering ($\alpha = 0.35$) was chosen to have RF bandwidth satisfy the Nyquist sampling criterion (1). The RF carrier was set to 2.40125 GHz according to (2). The whole setup therefore appeared to have a superheterodyne configuration.

Quadrature digital downconversion to baseband, demultiplexing into multiple channel data streams and matched filtering was done by offline processing. The

demultiplexed signals with inputs on all channels except Ch3 (which was terminated in 50Ω) are shown in Fig. 6. Some amount of leakage from the other channels is seen in the Ch3 data path. Also the presence of additional -4 dB power splitters on the Ch1 and Ch2 signal paths are reflected in their lower signal levels compared to Ch0.

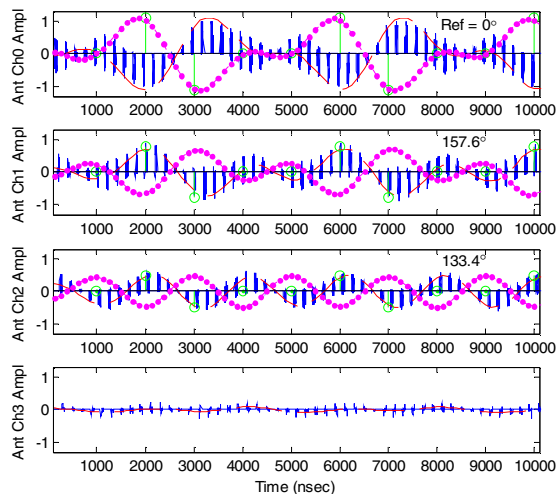


Fig. 6. Quad. Path Waveforms (O: Expected Symbols, •: Phase Rotated, --: Before Phase Rotation, Pulsed: Demuxed Signals).

Timing, frequency and phase synchronization was then established to recover the transmit data and determine the signal characteristics. The phase offset determined based on the known original data was used to rotate the complex baseband data on each of the channels. They are shown in Fig. 6 with each channel's carrier phase offset normalized to reference Ch0, i.e. rotated with the phase offset factor for Ch0. Phase/amplitude differences between channels was thus directly inferred from this processed data and compared with the known values introduced in the experimental setup. The results of one such comparison are presented for easy visualization in Fig. 7 in the form of symbol constellation diagrams for each channel with phase offsets seen in relation to reference Ch0. In this case, the phase rotations calculated were 16.4° and 25.2° on Ch1 and Ch2 respectively. The computed rotation values in the considered test cases were within the 5° of the actual phase shifter settings. These experiments confirmed that the system could track phase variations between channels well enough for the multiplexing architecture to prove useful in multi-antenna systems. Interference among the multiplexed channels is an important source of error in such time division multiplexed systems. The phenomenon is similar to the ISI problem encountered in digital communications. The available bandwidth as determined by any filtering action present in the multiplexed signal path is the cause of this

inter-multiplexed-channel interference. In this work, the 40 MHz IF filter is the bandwidth limiting component.

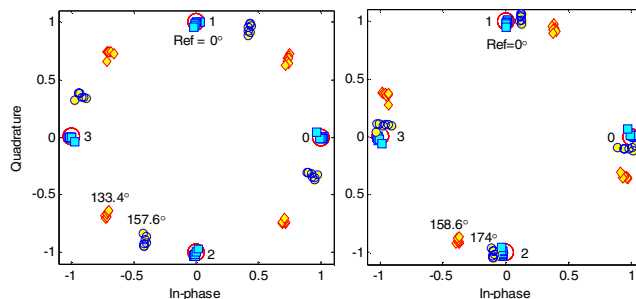


Fig. 7. Measurement comparison of two sets of per-channel symbol constellations with channel phase offsets normalized to Ch0 showing phase rotation on Ch1 and Ch2 (O: Expected Original Symbol, •: Ch0, •: Ch1, •: Ch2).

V. CONCLUSION

A new approach for dealing with multiple input RF channels in integrated multi-antenna receivers is introduced. This approach emphasizes circuit reuse for area and power savings by multiplexing the RF signal path right from the antenna front-end onwards. A prototype amplifier circuit that can handle up to 4 RF inputs of 2.4 GHz carrier frequency is integrated along with necessary switch drive buffers and digital controller functions in a $0.18 \mu\text{m}$ RF-CMOS process. The system was shown to correctly recover signal phase/amplitude information on a per input channel basis.

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