

## 15.6 Direct Conversion Dual-Band SiGe BiCMOS Transmitter and Receive PLL IC for CDMA/WCDMA/AMPS/GPS Applications

Kevin Gard, Kenneth Barnett, Jeremy Dunworth, Tony Segoria, Brett Walker, Jianjun Zhou, David Maldonado, Andrew See, Charlie Persico

Qualcomm, San Diego, CA

The proliferation of digital mobile telephone systems in the US, Europe, Japan, and Korea created a large demand for low cost high performance handsets. The radio frequency (RF) transceiver portion of the mobile phone is a significant portion of the overall cost, and the transceiver cost is proportional to the total number of components. The most expensive transceiver components are VCOs, filters, duplexors, power amplifiers (PA), and integrated circuits. Traditional mobile phone architectures use the super heterodyne architecture using two levels of frequency conversion [1], [2]. Filtering at both levels of frequency conversion enhances frequency selectivity; however, this requires external LC or SAW filters at the intermediate frequency and a linear IF to RF upconverter. Direct conversion architectures eliminate the intermediate frequency (IF) conversion and filtering steps resulting in the elimination of the IF filters and a reduction in current consumption for the transmitter implementation.

Reverse link power control (mobile to base station) and transmitter efficiency are two important aspects for CDMA/WCDMA mobile transmitters [3]. Mobile station output power is continuously changing according to the signal strength the base station receives. This requires the mobile station transmitter to support a gain control range of greater than 85dB. In super heterodyne architectures the dynamic range is divided between the IF and RF sections of the radio; however, for direct conversion most of the dynamic range is achieved at RF frequencies. The difficulty for a direct-conversion transmitter is that the local oscillator signal is at the same frequency as the RF output signal. When operating at reduced output power levels, the LO can leak to the RF signal path through the substrate and degrade carrier suppression performance.

This transmitter RFIC is designed for operation in the cellular CDMA/AMPS, JCDMA, KPCS, PCS, and IMT frequency bands. CDMA, AMPS, CDMA2000, and WCDMA modes of operation are supported. The RFIC is implemented as a single chip produced using a 0.4 $\mu$ m SiGe BiCMOS technology. The design includes an integrated transmitter with one output for cellular and two outputs for PCS/IMT band operation. In addition, the RFIC includes an integrated receiver PLL supporting cellular, PCS, and GPS bands. The direct-conversion transmitter architecture includes separate RF up-converters, variable gain amplifiers (VGA) for CELL and PCS/IMT bands, and individual driver amplifiers for each RF output as shown in Fig. 15.6.1. Integrated VCO, PLL, and frequency conversion circuits provide quadrature local oscillator (LO) signals to the up-converters. The only external passive components required are the transmit and receive PLL loop filters, output matching capacitors (one cap per output), one bias resistor, two capacitors for a baseband filter, and power supply bypass capacitors. Each mode of operation of the transmitter and receive PLL is controlled by software programming via a three-wire serial bus interface (SBI).

The direct-conversion transmitter achieves over 90dB gain control range by splitting up the gain control between the RF VGA, driver amplifier, and baseband input signal. Transmitter efficiency is controlled by adjusting the bias in accordance with the

gain control signal. A simplified circuit schematic of the driver amplifier is shown in Fig. 15.6.2. The RF output transistor (Q1) is biased class AB to maintain good efficiency while meeting the adjacent channel power rejection (ACPR) distortion requirements. Measured ACPR and power supply current consumption results are shown in Fig. 15.6.4. Plots of the gain control and gain slope curves are shown in Fig. 15.6.3.

Reducing bias current to the output device increases the output impedance to unacceptable levels that can disturb the frequency response of the SAW filter causing excessive insertion loss and increased gain slope across the pass band. At lower output power levels, a shunt AC resistance (R1) is slowly switched in using a MOSFET (M1) to keep the VSWR below 3:1 over the full output dynamic range. Measured VSWR results are shown in Fig. 15.6.4. The added shunt resistance coupled with attenuation provided by the output device improves LO leakage suppression at low output power. The output device is matched to 50 ohms using an integrated shunt inductor and a off-chip series capacitor. The differential voltage output of the VGA is converted to single-ended power drive to the output device using a stacked common-source common-emitter totem pole stage.

Extensive measurements of production parts ensure the RFIC meets the system requirements for CELL/AMPS and PCS modes of operation over the specified output power range. Figure 15.6.4 summarizes the typical measured transmitter performance compared against the system specifications for CELL and PCS bands of operation. The power supply measurement includes the sum of the transmitter signal path, PLL, VCO, and the receive PLL. The device operates over a 2.7V to 3.0V dc supply voltage and an ambient temperature range of -30°C to +85°C. The integrated transmitter VCO and PLL meet the closed-loop phase noise and spurious requirements of both AMPS and CDMA modes of operation. Typical closed-loop phase noise performance for CELL and PCS is shown in Fig. 15.6.5. The die area is 2.4mm x 3.25mm, and is packaged in a 6mm x 6mm BCC 40-pin chip-scale package. A die micrograph is shown in Fig. 15.6.6.

### Acknowledgements

The authors would like to thank A. Talmadge, C. Gorham, K. Zhang, J. Freville and E. Krommenhoek for layout design, S. Bar, H. Nguyen, and Eric Li for test support, and D. Laube and D. Martel for program management of the project.

### References

- [1] K. Sahota, et al., "A Base-Band to RF BiCMOS Transmitter RFIC for Dual-Band CDMA/AMPS Wireless Handsets," *2000 IEEE Radio Frequency Integrated Circuits Symposium Digest*, pp. 129-132.
- [2] M. Reddy, et al., "Highly Integrated, Dual Band/Tri-Mode SiGe BiCMOS Transmitter IC for CDMA Wireless Applications," *2002 IEEE Radio Frequency Integrated Circuits Symposium Digest*, pp. 35-38.
- [3] TIA/EIA IS-95-B, Mobile Station-Base Station Compatibility Standard for Dual-Mode Spread Spectrum Systems, October 1998.

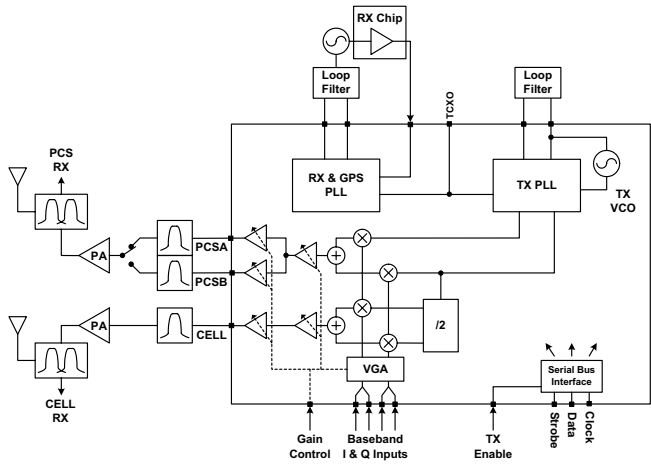


Figure 15.6.1: Dual-band CDMA transmitter architecture.

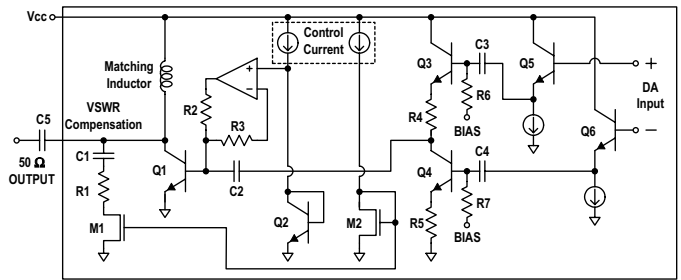


Figure 15.6.2: Driver amplifier schematic diagram.

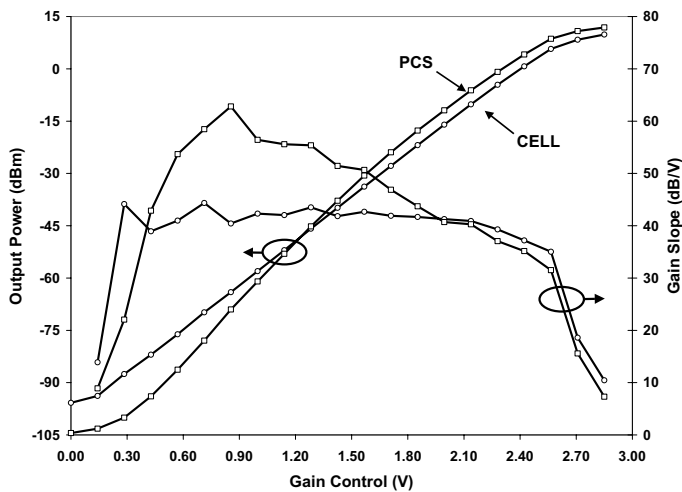


Figure 15.6.3: Gain control and gain slope.

Cellular Performance / Specification											
Output Power (dBm)	ACPR (dBc 1.23MHz/30kHz)		RX BAND Noise (dBm/Hz)		Carrier Suppression (dBc)		Image Suppression (dBc)		VSWR		Total Supply I <sub>dd</sub> (mA)
	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	
10	-55.8	-52.0	-133.4	-130.0	-54.9	-35.0	-41.9	-35.0	1.53	3.0	80.2
8	-55.1	-52.0	-134.9	-132.0	-55.0	-35.0	-41.9	-35.0	1.61	3.0	70.7
0	-55.0	-52.0	-140.0	-137.0	-54.1	-35.0	-41.6	-35.0	2.10	3.0	57.4
-30	/	/	/	/	-48.5	-35.0	-41.1	-35.0	2.49	3.0	44.5
-80	/	/	/	/	-15.5	-10.0	-36.5	-25.0	2.48	3.0	40.2
PCS Performance / Specification											
10	-56.2	-52.0	-132.5	-130.0	-48.2	-26.0	-32.6	-26.0	1.22	3.0	78.6
8	-57.3	-52.0	-133.7	-132.0	-48.2	-26.0	-32.5	-26.0	1.47	3.0	71.2
0	-54.9	-52.0	-138.7	-137.0	-47.3	-26.0	-32.3	-26.0	1.82	3.0	56.2
-30	/	/	/	/	-44.6	-26.0	-31.9	-26.0	2.51	3.0	42.4
-78	/	/	/	/	-18.9	-10.0	-28.9	-25.0	2.45	3.0	36.3

Figure 15.6.4: Cellular and PCS transmitter performance.

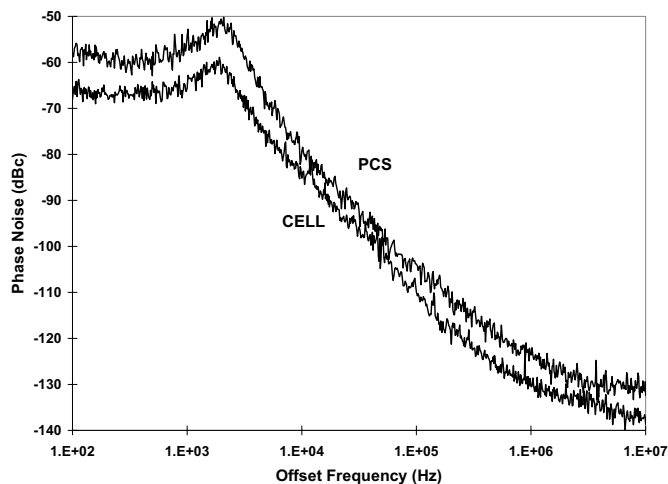


Figure 15.6.5: VCO and PLL closed loop phase noise.

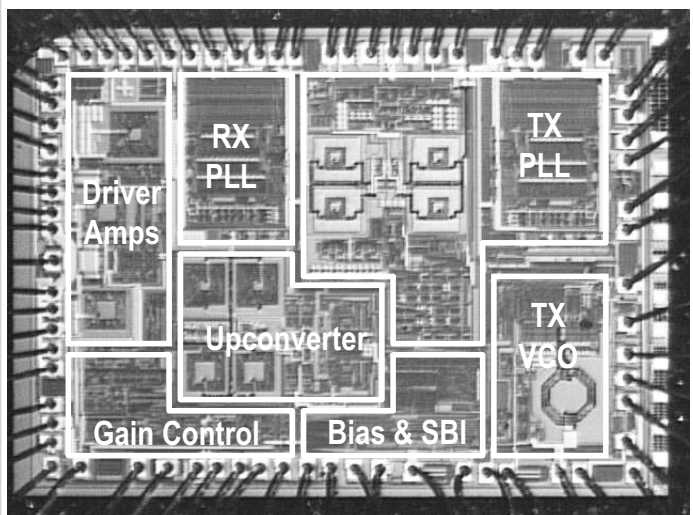


Figure 15.6.6: Die micrograph.

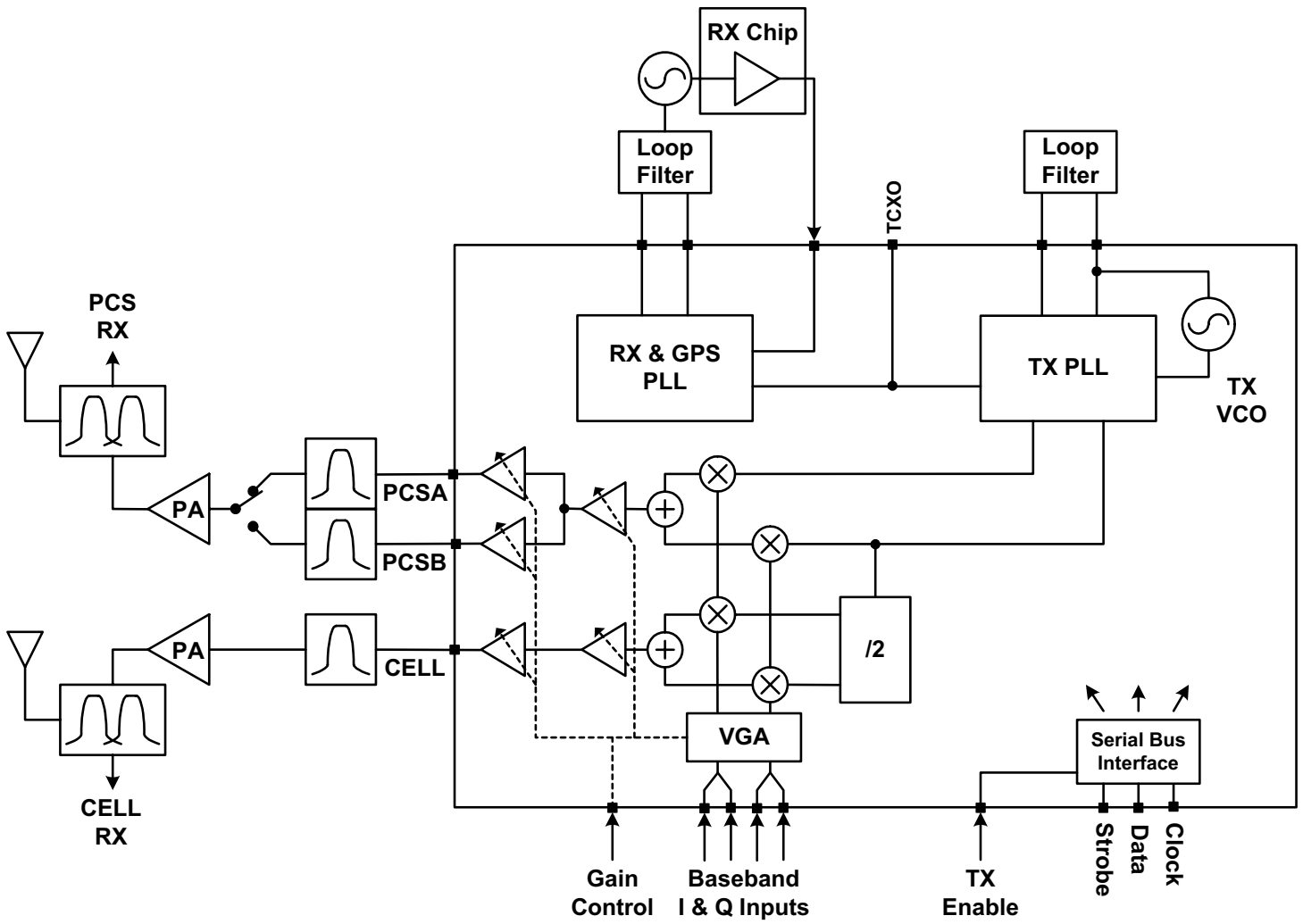


Figure 15.6.1: Dual-band CDMA transmitter architecture.

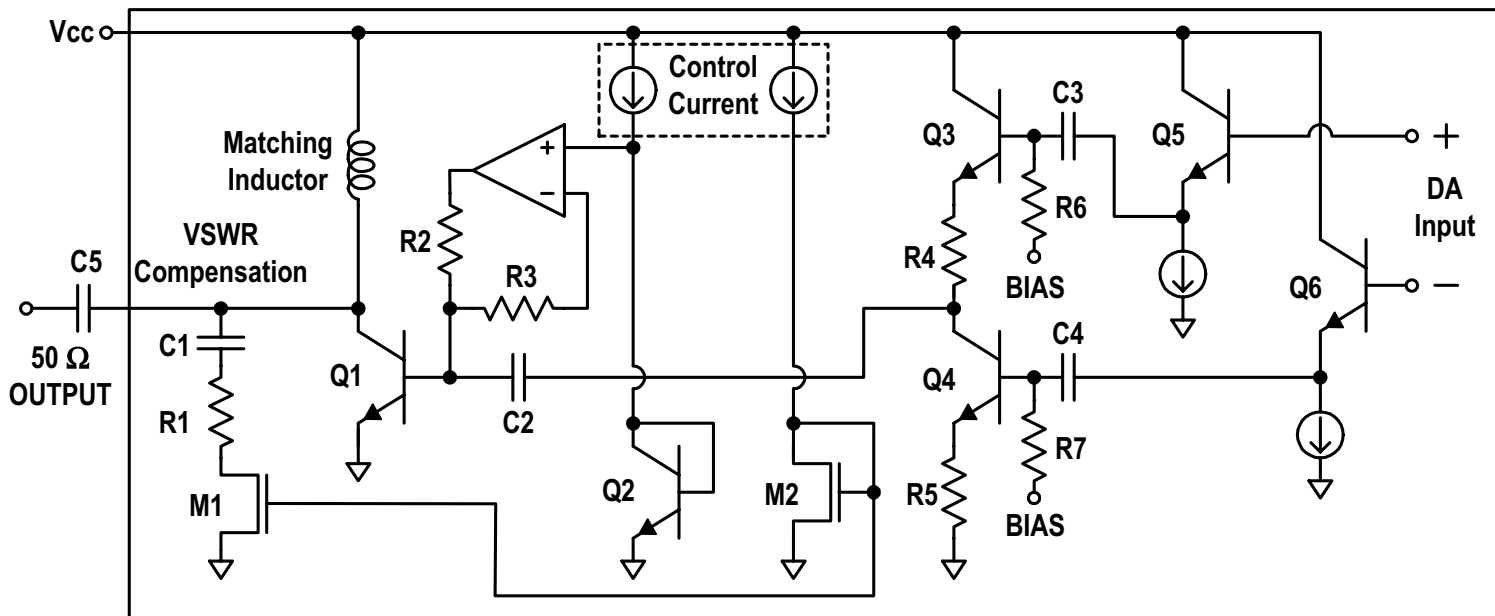


Figure 15.6.2: Driver amplifier schematic diagram.

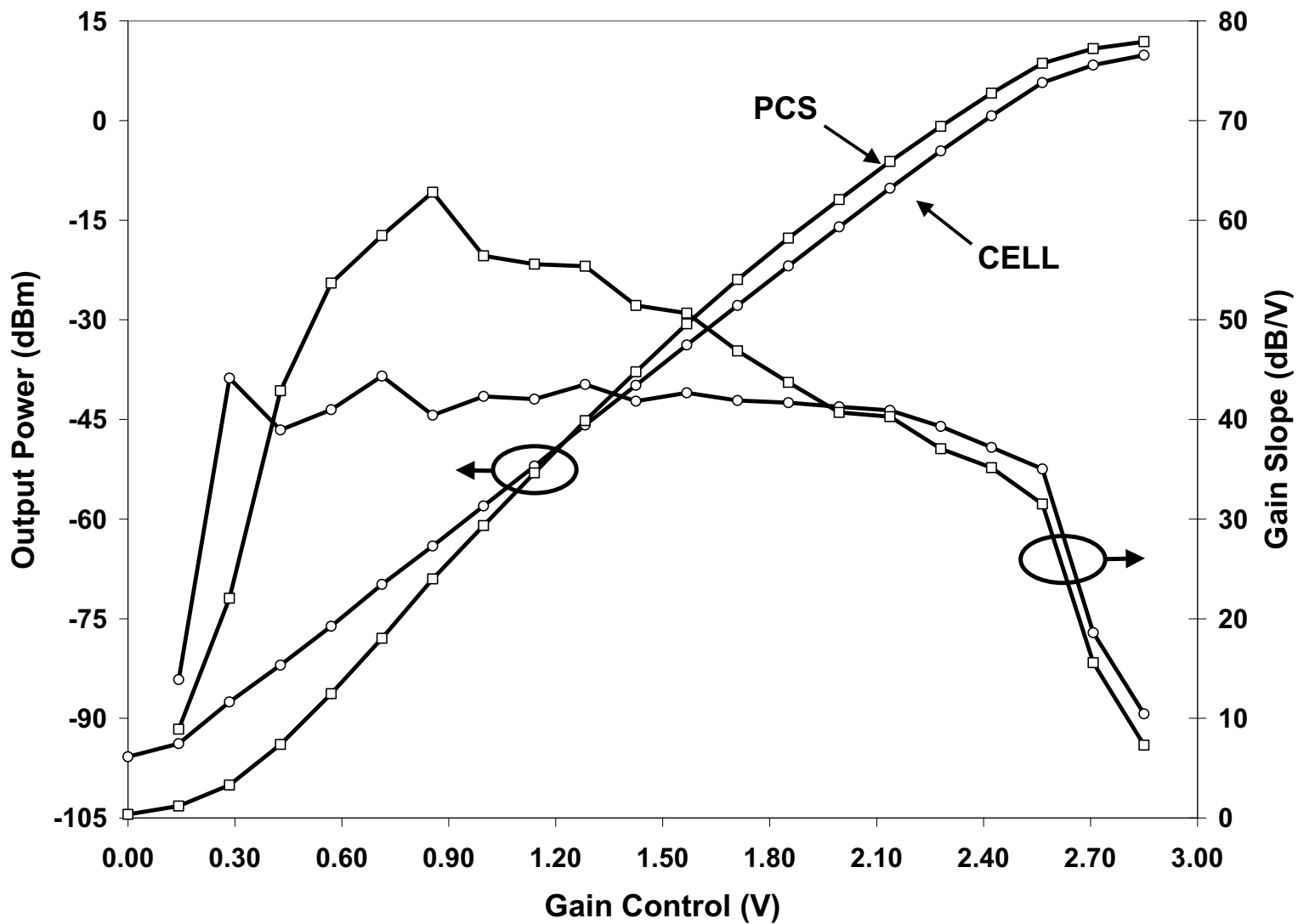


Figure 15.6.3: Gain control and gain slope.

Cellular Performance / Specification											
Output Power (dBm)	ACPR (dBc 1.23MHz/30kHz)		RX BAND Noise (dBm/Hz)		Carrier Suppression (dBc)		Image Suppression (dBc)		VSWR		Total Supply Idd (mA)
	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	Meas.	Spec.	
10	-55.8	-52.0	-133.4	-130.0	-54.9	-35.0	-41.9	-35.0	1.53	3.0	80.2
8	-55.1	-52.0	-134.9	-132.0	-55.0	-35.0	-41.9	-35.0	1.61	3.0	70.7
0	-55.0	-52.0	-140.0	-137.0	-54.1	-35.0	-41.6	-35.0	2.10	3.0	57.4
-30	/	/	/	/	-48.5	-35.0	-41.1	-35.0	2.49	3.0	44.5
-80	/	/	/	/	-15.5	-10.0	-36.5	-25.0	2.48	3.0	40.2
PCS Performance / Specification											
10	-56.2	-52.0	-132.5	-130.0	-48.2	-26.0	-32.6	-26.0	1.22	3.0	78.6
8	-57.3	-52.0	-133.7	-132.0	-48.2	-26.0	-32.5	-26.0	1.47	3.0	71.2
0	-54.9	-52.0	-138.7	-137.0	-47.3	-26.0	-32.3	-26.0	1.82	3.0	56.2
-30	/	/	/	/	-44.6	-26.0	-31.9	-26.0	2.51	3.0	42.4
-78	/	/	/	/	-18.9	-10.0	-28.9	-25.0	2.45	3.0	36.3

Figure 15.6.4: Cellular and PCS transmitter performance.

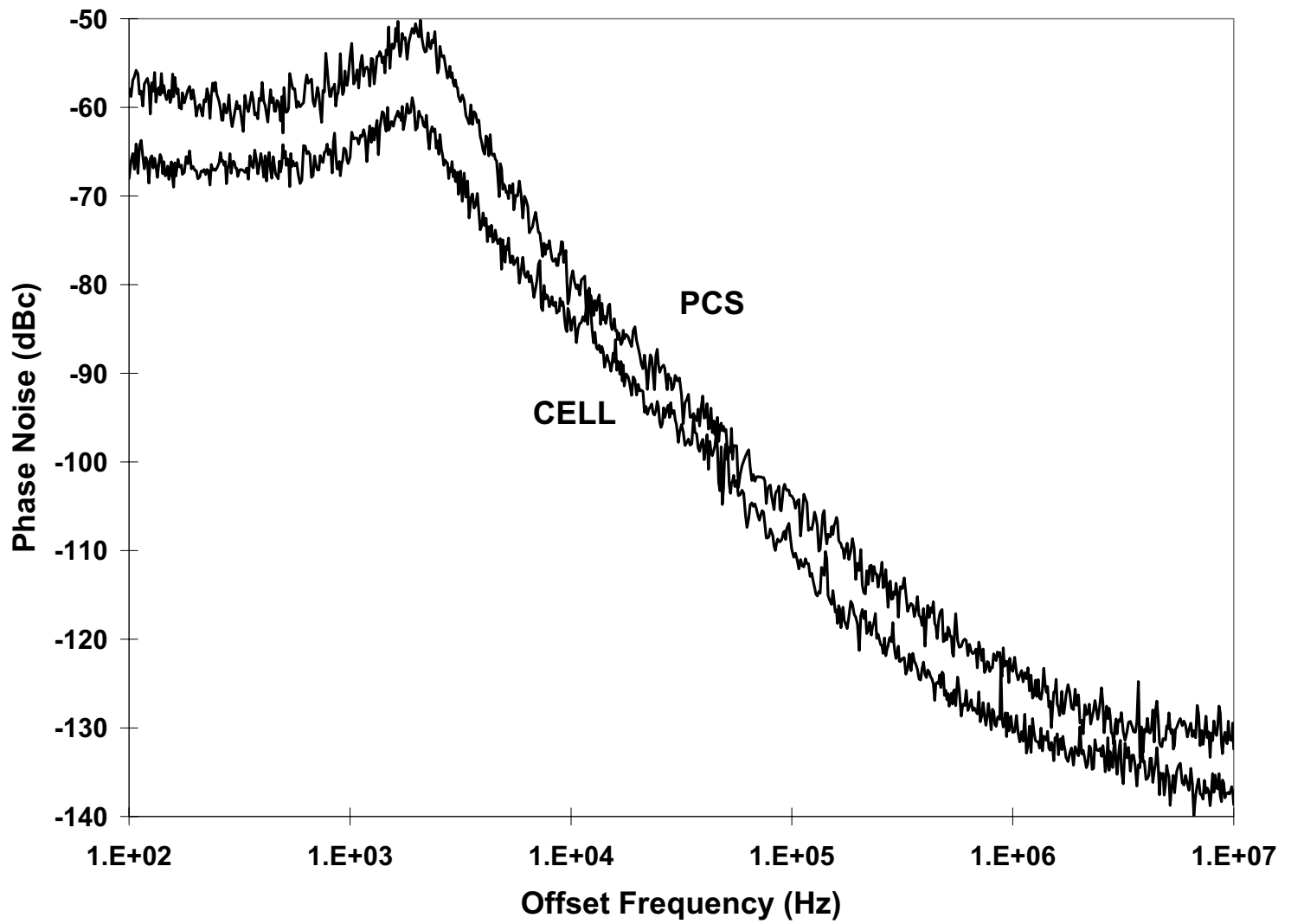


Figure 15.6.5: VCO and PLL closed loop phase noise.

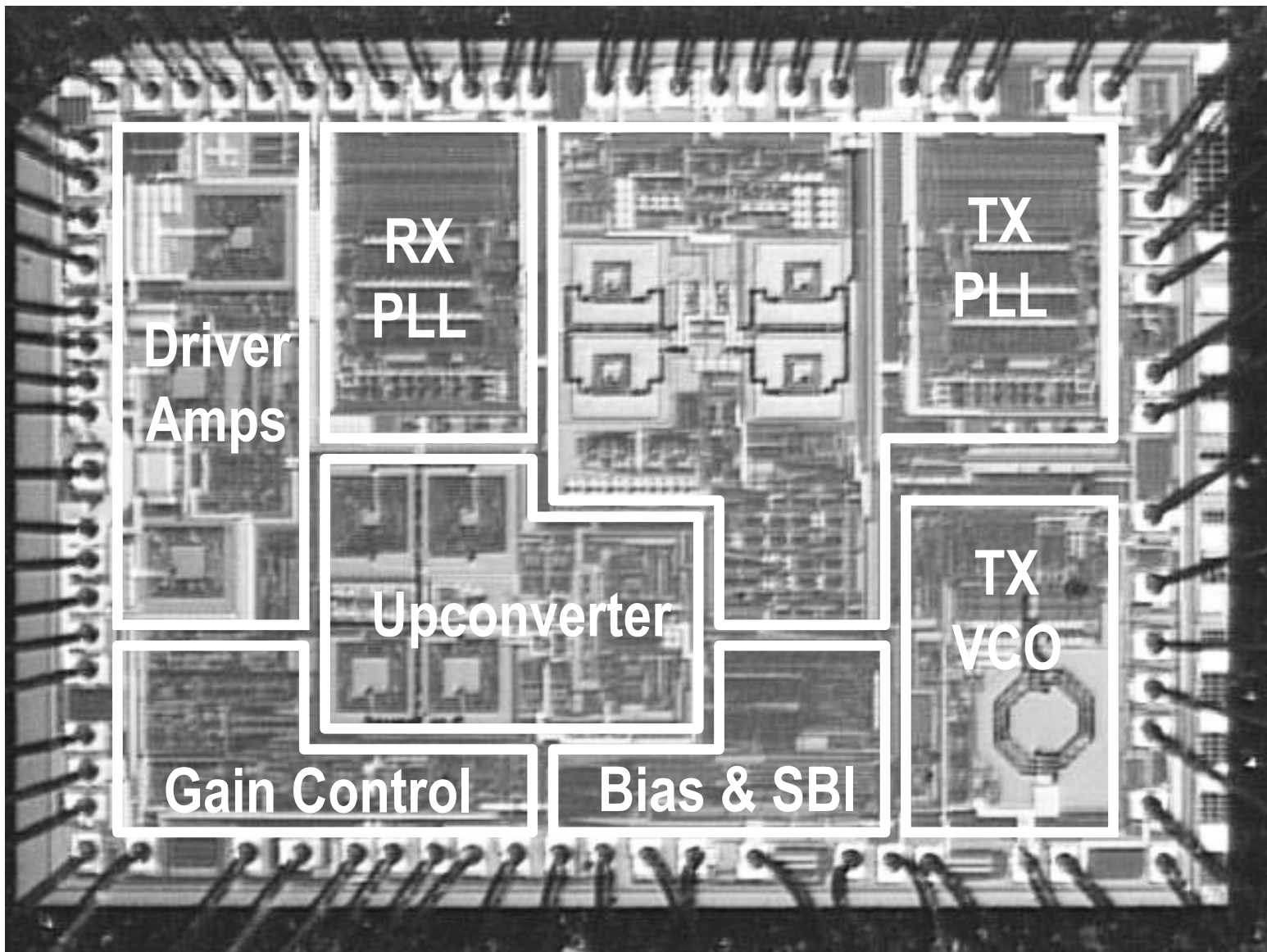


Figure 15.6.6: Die micrograph.