10MHz Current Mode 4 Switch Buck Boost Converter (4SBBC) for Polar Modulation

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***Abstract*— This paper presents a transistor level design of a current mode 4 switch buck boost converter (4SBBC) for polar modulation. The reference signal of this 4SBBC is the envelope signal of EDGE (Enhancement Data-rate for GSM Evolution) standard which has more than 200kHz bandwidth. In order for output voltage to follow this fast varying reference signal, this 4SBBC uses current mode control with 10MHz fixed switching frequency which demands high bandwidth circuit design. This paper will show how to design the high speed current sensor and oscillator well operating with 10MHz switching frequency. The current sensor exhibits rail to rail input and output range, and active feed back scheme makes it work well in 10MHz switching frequency range. The oscillator generates 2 sawtooth signals which have precise and stable 180 degree phase shift each other by using common mode feedback scheme. The transistor level simulation shows this 4SBBC converter has more than 80% average efficiency with real EDGE envelope reference and is capable of wide input, output voltage range which is suitable for EDGE polar modulation.**

I. INTRODUCTION

High efficiency RF power amplifiers (RF PAs) are critical in portable battery-operated wireless communication system because they dominate the power consumption of the system. Especially, EDGE system uses the envelope varying signal to increase its data rate. This envelope variation requires the linear or linearized RF power amplifier. However, linear power amplifiers, such as class A, class B or class AB have a drawback of low efficiency which degrades battery run time [1].

One popular architectural solution to transmit envelope varying signal with high efficiency is the polar modulation which is shown in Fig. 1 [1]–[5]. Polar modulation uses two signal paths; one is envelope path, *A(t)*, and another is phase path, $\phi(t)$. This phase path contains no envelope variation, so high efficient nonlinear power amplifier such as Class E can be used to transmit phase information. Then the envelope variation is restored by modulating the supply voltage of power amplifier through the envelope path.

In this paper, we will propose 4SBBC to be used as a envelope modulator for polar modulation. First, the principle of polar modulation and EDGE signal are reviewed in section II. In Section III, the design of the current mode 4SBBC is discussed. Here, we will talk about the implemetation of double edge current mode control, current sensor and oscillator in detail. In section IV, several simulation results will be shown such as time domain, spectrum mask simulation and average efficiency by applying the EDGE signal to the reference of the DC/DC converter.

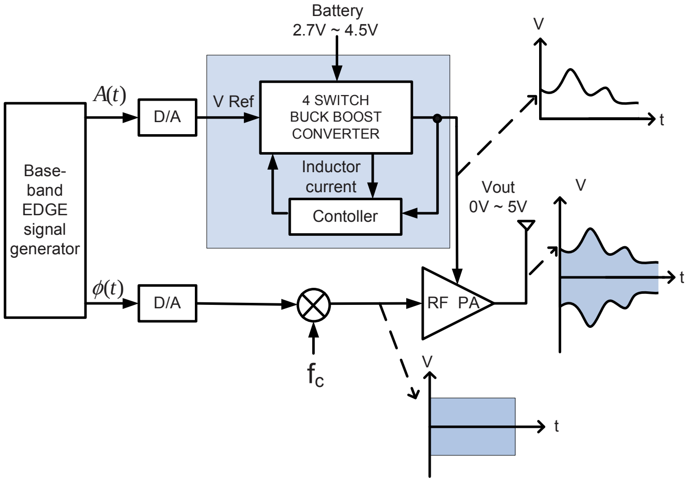

Fig. 1. Block diagram of polar modulation with buck boost converter as a envelope modulator

II. THE SUMMARY OF POLAR MODULATION AND EDGE STANDARD

A. Polar Modulation

The block diagram of typical polar modulation is shown in Fig. 1. In this figure, the envelope modulator is implemented with 4SBBC. The essense of polar modulation is separating the envelope signal, *A(t)* and phase signal, $\phi(t)$ from transmitting information. In polar modulation, the power amplifier is only processing phase modulated signal which has a constant envelope. This means the power amplifier do not need linear amlification. So a switched mode power amplifer such as class E can be used in this system whose power consumption is theoretically zero [1], [6]. The time varying envelope signal is recombined at power amplifier by modulating supply voltage through the envelope modulator. Now the linearty of the transmitter depends on the linearity of the envelope modulator. Any conventional power supply

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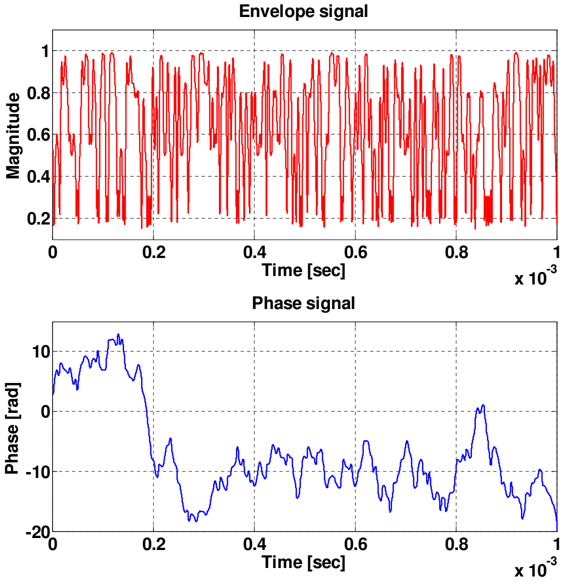

Fig. 2. EDGE signal in time domain (provided by RFMD)

like linear regulator or switched mode power supply can be used as a envelope modulator, even if the response of the power supply from Vref to Vout has linear relationship, and the loop gain is wide enough to envelope signal bandwidth. Even to the envelope modulator, switched mode power supply has theoretically 100% power efficiency. So with polar modulation architecture, both high efficiency and high linearity can be achieved if we have a good enough enveope modulator.

B. EDGE Signal

In order to design the envelope modulator properly in polar modulation architecture, the understanding of the signal which will be used in this system is necessary. In this paper, we will use EDGE standard as a transmitting signal.
A EDGE standard is the evolution of the current GSM standard to provide higher bit rates of 812.5kbps by using $3\pi/8$ offset 8–PSK as opposed to GSM bit rates of 270.8kbps, which use GMSK modulation. The symbol rates of EDGE is equal to the bit rate of GSM because in EDGE mode, each symbol represents 3 bit [4], [7]. Fig. 2 shows the EDGE signal in time domain. Fig. 2(a) is the envelope signal waveform $A(t)$ and Fig. 2(b) is the phase signal waveform $\phi(t)$ in time domain respectively. The envelope variation in EDGE system is 17dB peak to minimum ratio, and this corresponds to voltage variation of 0.706V to 5V. This means the proposed envelope modulator must have wide output voltage range, regardless of input voltage variation.
Another feature of the EDGE signal can be revealed by its frequency domain information. Fig. 3 shows the the envelope and phase components of EDGE signal with composite complex EDGE signal and transmit mask together. As shown in Fig. 3, the composite complex EDGE signal has most energy within 200KHz offset from center frequency. However, envelope and phase signal has wider spectrum than composite complex EDGE signal spectrum. Several papers discussed this issue and proposed different bandwidths for envelope and phase path which are around 1–2 MHz. [4], [5].

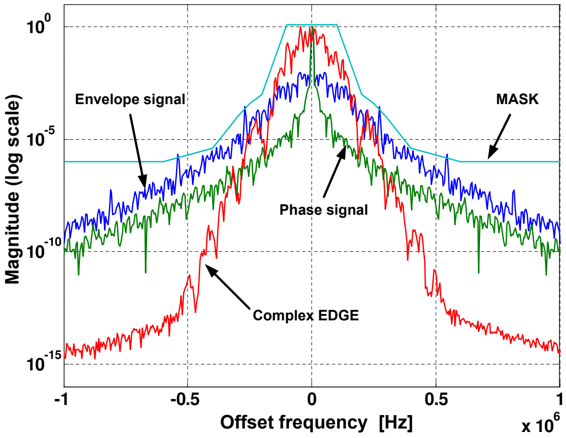

Fig. 3. EDGE signal in frequency domain

III. DESIGN DETAILS

Based on the information we discussed in section II, we can set up the design parameters for 4SBBC which will be used as a envelope modulator in polar modulation. Fig. 4 shows the block diagram of the current mode 4SBBC. In order to cover wide output voltage range of 17dB peak to minumim voltage with 2.7V – 4.5V of battery voltage, we choose the buck boost scheme as a power stage. As you know, the buck boost converter can generate higher or lower voltage than input voltage. We adopted current mode method for controlling this 4SBBC. Current mode control scheme can give us a faster response and easier design of compensator than voltage mode control which is suitable to process fast EDGE enveope signal with high stability [8]. The table I shows the summary of the design parameters of the 4SBBC with appropriate compensator. The worst case in tabel I means the boost mode when Vin=2.7V and Vout=5V. With 10MHz switching frequency, the worst case bandwidth (from Vref to Vout) of the 4SBBC is around 2MHz as shown in Fig. 5.

A. Double Edge Current Mode Control

For controlling the 4SBBC, we used the current mode control scheme. The current mode control makes the two pole response of the power stage (which is generally from L,C output filter) into single pole response system effectively. So it is relatively easy to design a controller that exhibits a well behaved response, having enough phase margin over a wide range of operating points [8]. These results tell that current mode control scheme is a good candidate for envelope modulator application.

$$Boost = (I_L + V_A) - V_C \tag{1a}$$

$$Buck = V_C - (I_L - V_A) \tag{1b}$$

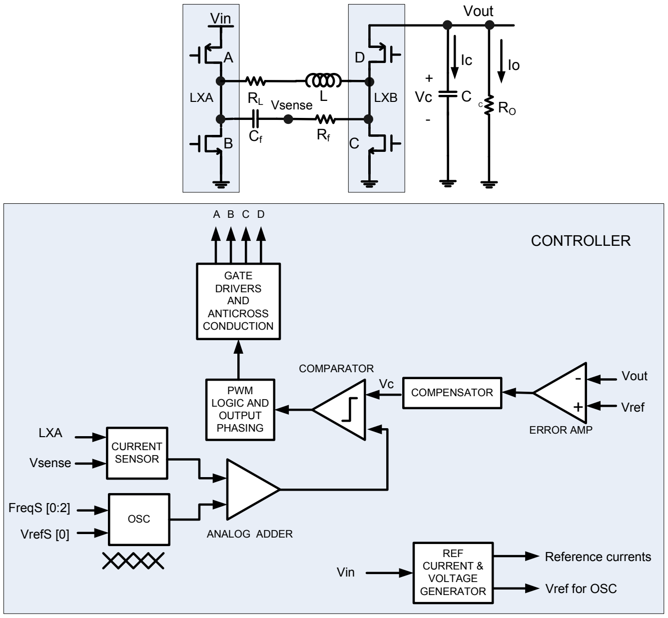

Fig. 4. Block diagram of 4SBBC with controller

TABLE I
DESIGN PARAMETERS FOR 4SBBC

Input voltage range	V_{in}	2.7V – 4.5V
Ouput voltage range	V_{out}	1V – 5V
Switching frequency	f_{sw}	10MHz
Output inductor	L	280nH
Output capacitor	C	250nF
Load resistor	R_o	5Ω
Output filter resonant frequency	$\frac{1}{2\pi\sqrt{LC}}$	602KHz
Worst case loop gain cutoff frequency	f_c	519KHz
Worst case Phase margin	degree	47.1
Worst case Closed-loop control bandwidth	B_{-3dB}	≈2MHz

In order to save the dynamic power losses, we seperate the control modes into buck mode and boost mode. By using this way, only a pair of power switches is working during one cycle; switch A and B for buck mode, and switch C and D for boost mode.

The Fig. 6 shows the conventional peak current control for boost mode (a) and valley current control scheme for buck mode (b). According to the above control methods, the decision equations for buck and boost mode are described in the Equ. 1.

$$Boost_{on} = (I_L - V_A) - V_C \tag{2a}$$

$$Boost_{off} = (I_L + V_A) - V_C \tag{2b}$$

$$Buck_{on} = V_C - (I_L - V_A) \tag{2c}$$

$$Buck_{off} = V_C - (I_L + V_A) \tag{2d}$$

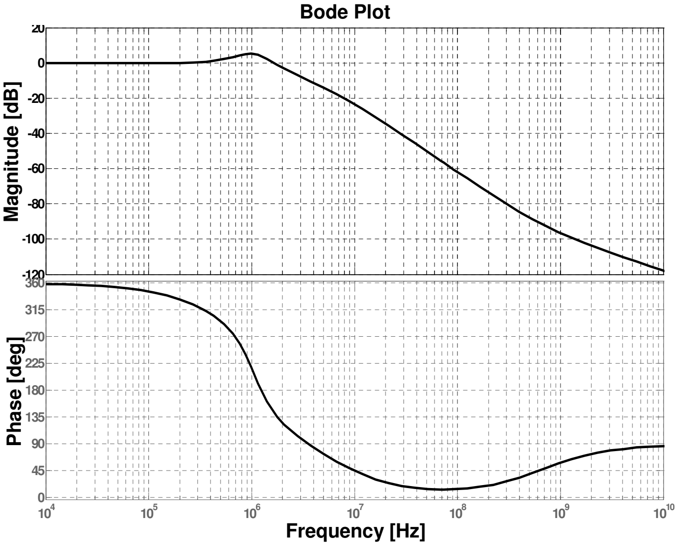

Fig. 5. Closed loop response of 4SBBC from Vref to Vout @ Vin=2.7 and Vout=5V

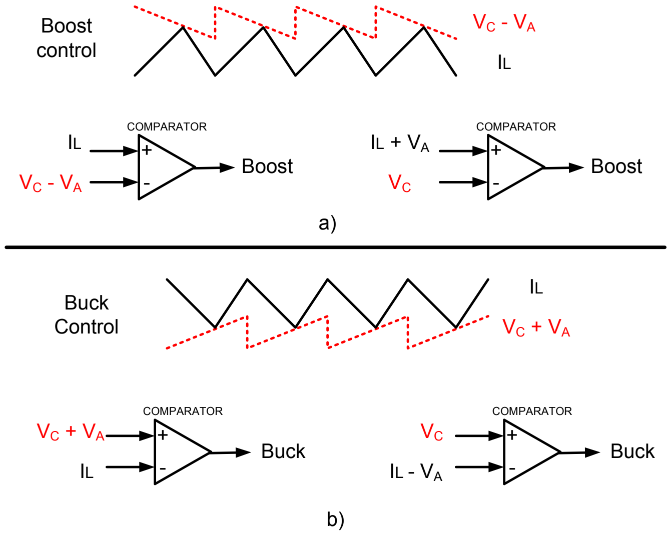

Fig. 6. Conventinal cunrrent mode control

In order to improve the reponse of the control, we used a double edge current mode control scheme which means turn-on and turn-off time of the switches are determined by valley-current control and peak-current control respectively [9]. The Fig. 7 shows the conceptual scheme of double edge current mode control methods for both boost mode (a) and buck mode (b). The decision equations for buck and boost mode are described in the Equ. 2.

As shown Fig. 7, we need sawtooth waveform (V_A) which is required to make the system stable when duty cycle is higher than 0.5 [8]. Because we use double edge modulation scheme, we need double sides sawtooth waveform which are expressed as V_A and $-V_A$. Also we need two sawtooth waveforms for buck and boost mode respectively which does not have any

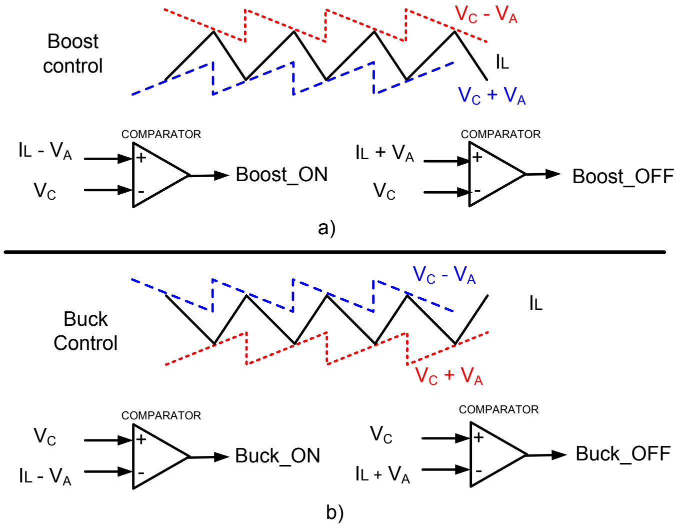

Fig. 7. Double edge current mode control

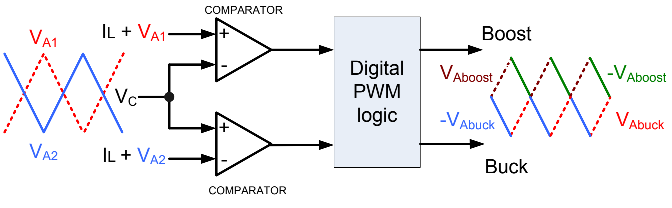

Fig. 8. PWM logic for currnet mode control

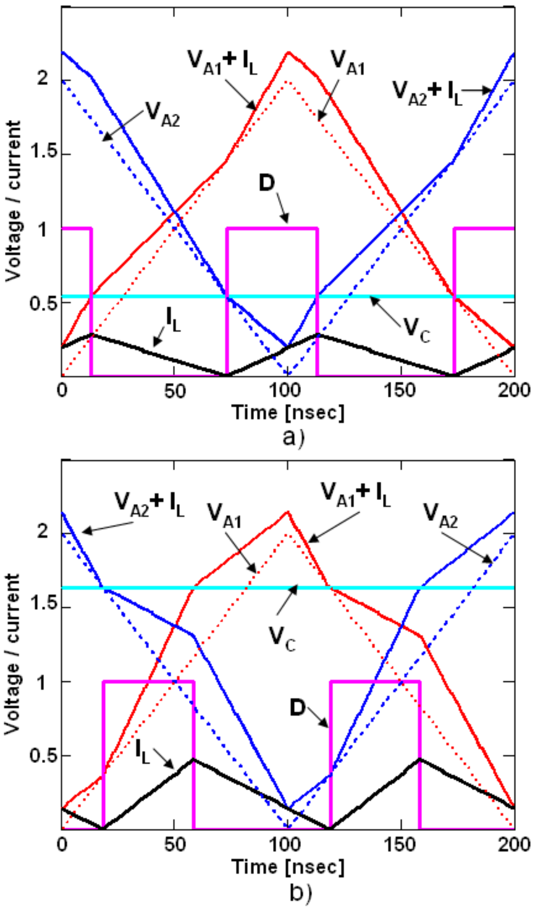

Fig. 9. Key signals of double edge current mode control a) Buck mode with D=0.4 b) Boost mode with D=0.4

overlap. No overlap guarantees that the 4SBBC works as only either buck or boost mode to save dynamic power loss.

However, to generate exactly touching two sawtooth waveforms is not easy, because some components variation in the chip with respect to temperature and operating points make it easy for the sawtooth waveforms to have either overlap or non-touching. The Fig. 8 shows one method to solve this. We can generate 100% overlapped sawtooth waveforms (V_{A1}, V_{A2}) before adding inductor current information (I_L) with those. By using digital logic block, we can make the two sawtooth waveforms work as exactly touching waveforms. Then the each sides of sawtooth waveforms correspond to $V_{Abuck}, -V_{Abuck}, V_{Aboost}$ and $-V_{Aboost}$ which can be directly applied to the Equ. 2.

Fig. 9 shows the key waveforms to explain the double edge current mode control scheme used in this paper. Fig. 9 (a) is for buck mode and Fig. 9 (b) is for boost mode. Both are when duty cycle is 0.4. As shown in Fig. 9, the duty cycles are modulated in both edges.

B. Current Sensor

In order to sense the continuous current information, we used the “Filer-Sense the inductor” technique [10]. This technique uses a RC network (R_r, C_r) to filter the voltage across the inductor and sense the current through the equivanlant series resistance (ESR, R_L) of the inductor as shown in Fig. 4. The design equation is shown in Equ. 3.

$$V_{C_r} = V_{sense} = I_L \cdot R_L \tag{3a}$$

$$\text{, where} \quad \frac{L}{R_L} = R_r \cdot C_r \tag{3b}$$

To sense the inductor current information by using above technique, there are two major design issues. One is wide voltage swing at LXA and Vsense nodes in Buck mode. During the buck mode operation, power switch A and B are operating in each cycle, so the voltage at LXA and Vsense nodes change from Vin to ground and vice versa. To sense the differential voltage across the C_r with such a wide common mode voltage change, the input stage of the current sensor should cover the rail to rail common mode range. This can be achieved by using PMOS and NMOS differential pairs together in input stages.

Another design issue is that wide bandwidth of the current sensor is reqired. The switching frequency used here is 10MHz. To sense such a high frequency current information without distortion, we need a high speed current sensor scheme. We desighed such a high speed current sensor by using active

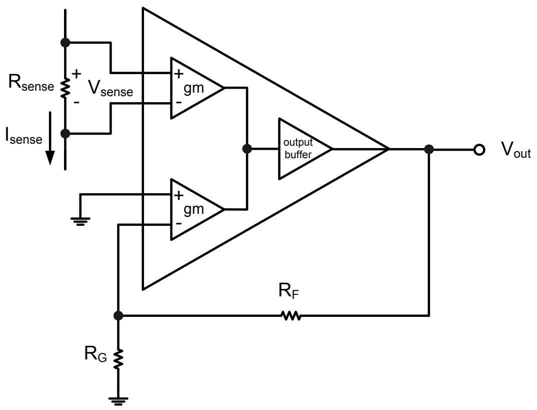

Fig. 10. Current Sensor by using Active Feedback Amplifier [11], [12]

feedback amplifier (AFA) architecture which is shown in Fig. 10 [11], [12].
The AFA provides a benefitial separation between the signal input and the feedback network. The brief operation of AFA is like following. Because of the infinite input impedance of output buffer in AFA, all current generated by the G_m block which senses the V_{sense} flows into output node of another G_m block. This makes the input voltage of the bottom G_m block copy the same voltage as V_{sense} but with different polarity if those G_m blocks are identical. This copied voltage will be applied across the R_G and amplifed to V_{out} which corresponds to Equ. (4). The CADENCE simulation shows that the 3dB bandwidth of this AFA is more than 20MHz for rail-to-rail input voltage range.

$$V_{out} = \left(1 + \frac{R_F}{R_G}\right) \cdot V_{sense} \tag{4}$$

C. *Sawtooth Generator; Oscillator*

To implement the double edge current mode control explained in section III-A, we need two double side sawtooth signals which are 180^o phase shifted each other and keep the maximum and minimum values of each signals same. The Fig.11 shows the block diagram of the sawtooth generator performing the functions mentioned just above. Because we need double side sawtooth waveforms, the sawtooth generator has two current sources (I_1 and I_2). The capacitors are charged and discharged with these two current sources. The M_1, M_2, M_3 and M_4 work as a switch to chage the current path from V_{o1} or V_{o2}. When the voltage at either V_{o1} or V_{o2} reaches maximum voltage (V_H), the comparator (Comp) generates signals to switch the current path to V_{o1} and V_{o2} nodes. If the values of the current sources are not matched, the peak to peak voltage of V_{o1} and V_{o2} keep increasing or decreasing as time goes by. To solve this problem, we use common mode feedback (CMFB) scheme which forces to keep the average voltage of V_{o1} and V_{o2} to (V_M) which is half voltage of peak to peak sawtooth waveform. The frequency of this oscillator is determined by the Equ.(5). The FreqSA, FreqSB and FreqSC represent digital input pins used for changing the current value to vary frequency.

$$Frequency = \frac{I}{4 \cdot C \cdot (V_H - V_M)} \tag{5}$$

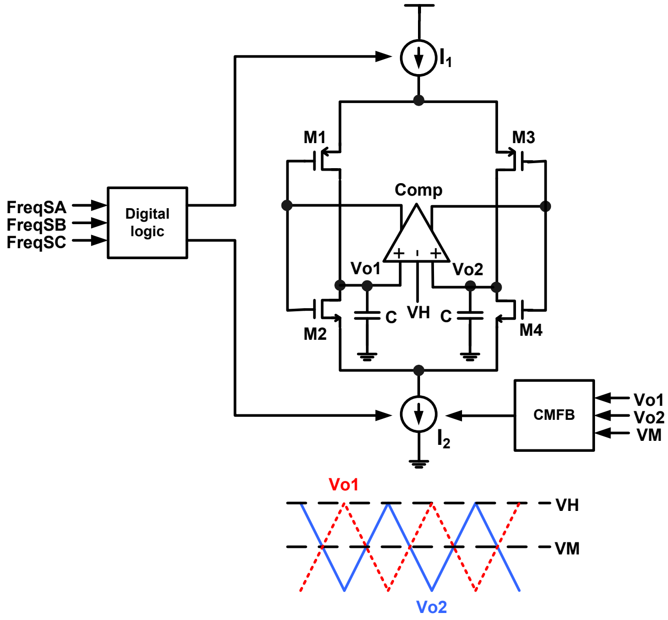

Fig. 11. Sawtooth generator

D. R_{DSon} *Effect to The System*

The 4SBBC works as buck mode or boost mode depending on the relationship between input and output voltage. Ideally the output voltage of boost converter can be infinite when the duty cycle at boost mode is close to 1. However, when we consider lossy parasitic components such as R_{DSon} and inductor ESR(R_{DSon}), the maximum voltage of boost converter is limited by those [8]. The case of 4SBBC working at boost mode is much worse than boost converter because the number of switches from input to output is more than boost converter. The Equ. 6 shows the effects of R_{DSon} in each switch and inductor ESR(R_{DSon}) to output voltage at boost mode in 4SBBC. From this Equ. 6, we can expect the effects of the R_{DSon} of switch A and inductor ESR(R_{DSon}) are dominant. As shown in the Fig. 12, we can see that if R_{DSon} of switch A or inductor ESR (R_L)is more than 0.4Ω, the output voltage of 4SBBC cannot reach to 5V with Vin = 2.7V. So when we integrate the power switches into chip, we should be careful to design the switch A.

IV. SIMULATION RESULTS

In this section, we will see some simulation results to verify the 4SBBC work with EDGE enveope. All simulation in this paper was done with JAZZ $0.5\mu m$ technology in CADENCE enviornment.

Fig. 13 shows the time domain simulation results of 4SBBC. For this simulation, we set the Vin is 3.3V and applied the

$$V_{out} = \frac{V_{in}}{(1-D)\Big(1+\frac{1}{(1-D)}\frac{R_D}{R_O}+\frac{1}{(1-D)^2}\big(D\frac{R_C}{R_O}+\frac{R_A+R_L}{R_O}\big)\Big)} \tag{6}$$

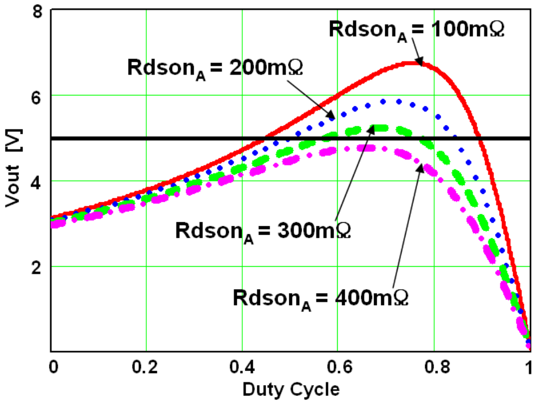

Fig. 12. Vout versus Duty cycle at boost mode with different Rdsons of A; Red(line): 0.1Ω, Blue(dot): 0.2Ω, Green(dash): 0.3Ω, Purple(dash-dot): 0.4Ω

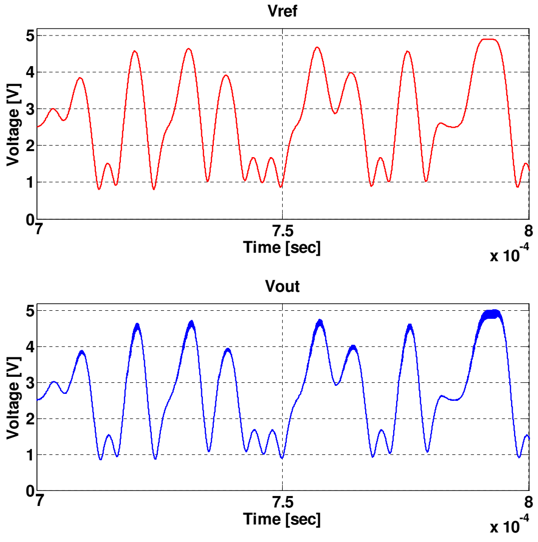

Fig. 13. Time domain simulation with EDGE envelope signal as a reference

EDGE enveolope signal to Vref of 4SBBC. As shown in Fig. 13, the output voltage of 4SBBC follows well the Vref and a distortion during the mode change from buck mode to boost mode or vice versa is not shown explicitly. However, the voltage ripple in boost mode is more than in buck mode.

Fig. 14 shows the spectrum mask simulation of the 4SBBC. Because the EDGE is complex signal, to plot this spectrum, we need to combine Vout with EDGE phase signal whice are real values. As shown in Fig. 14, the combination of Vout of 4SBBC and EDGE phase signal without delay compensation does not satisfy the spectrum mask. This is because the EDGE envelope signal experiences some delay through the 4SBBC and the delay mismatch between envelope signal and phase signal generates spectrum growth effect [2]. After adding delay to EDGE phase signal, output EDGE signal satisfy the spectrum signal mask. Table II shows the average efficiency of 4SBBC when 1msec long EDGE envelope signal is applied to Vref of 4SBBC. The simulation results show that more than 80% average efficiency with 10MHz switching frequency as shown in Table II. These simulation results prove that the proposed 4SBBC in this paper can be one of the candidate of the envelope modulator for EDGE polar modulation application.

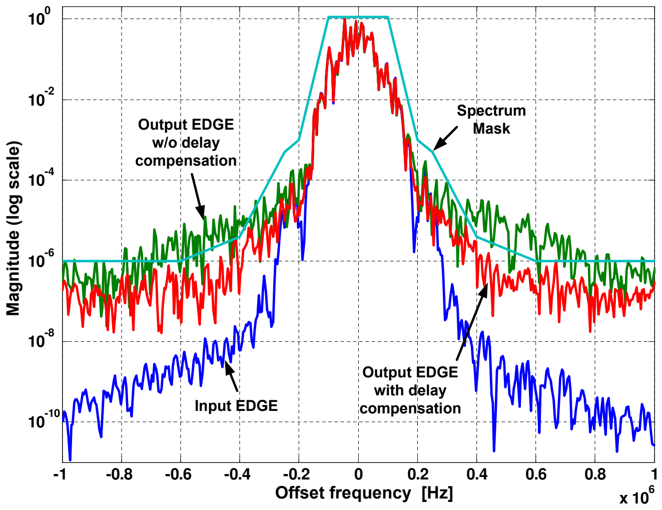

Fig. 14. Spectrum mask simulation

TABLE II

AVERAGE EFFICIENCY OF 4SBBC WITH 1MSEC LONG EDGE ENVELOPE SIGNAL

Frequency	V_{in}	Efficiency (η)
10MHz	3.3V	82.16%
10MHz	4.5V	85.47%
20MHz	3.3V	79.29%

V. CONCLUSION

In this paper, we reviewed the concept of the polar modulation which satisfy both the linearity and efficiency in transmitter system. The EDGE signal characteristic was analyzed in time and frequency domain.

A 10MHz current mode 4SBBC was proposed as a envelope modulator in polar modulation in this paper. To follow the fast EDGE enveoloe signal, this 4SBBC used double edge current mode control. A high bandwidth current sensor by using AFA was used, and sawtooth generator with CMFB was proposed. The time domain and spectrum mask simulation was used to show that the 4SBBC meets the EDGE mask standard and has more than 80% average efficiency with 1msec long EDGE envelope signal. The simulation results verify that the 4SBBC is a possible solution for this application.

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