ECE792X: Integrated Circuits for Wireless Communications
Sect. 005, Spring 2005

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Course web page
http://courses.ncsu.edu/ece792x/
******Please use the course bulletin board*** to ask questions about lectures, hw, projects, etc. It is the best way to broadcast questions that may be of interest to everyone.

Required text: Thomas Lee, ***The Design of CMOS Radio-Frequency Integrated Circuits***, Cambridge University Press. **2nd edition**.

Supplemental references (not required, but could be helpful)
Paul R. Gray and Robert G. Meyer, ***Analysis and Design of Analog Integrated Circuit***s, 4th edition, Wiley.
Bosco Leung, ***VLSI for Wireless Communications***, Prentice Hall, New Jersey, 2002.
Behzad Razavi, ***RF Microelectronics***, Prentice Hall, New Jersey, 1998.

Prerequisite: ECE711 Graduate introductory analog circuit course (ECE711: dc biasing, small-signal analysis of bipolar and CMOS circuits, multistage op amp design, stability and compensation, and current mirror biasing). Experience with DC, AC, and TRANS (transient) SPICE analysis of circuit designs.

Grading:
20% Midterm
30% Final exam
10% HW
40% Project

The following cutoffs (inclusive) will be used for letter grades: A+: 97%, A: 93%, A-: 90%, B+: 87%, B: 83%, B-:80%, C+: 77%, C: 73%, C-: 70%, D+: 67%, D: 63%, D-: 60%.

Course objectives: After taking this course, the student will be able to analyze, simulate, and design the key building blocks of an integrated radio: amplifiers, mixers, and oscillators. The students are exposed to some important topics of radio design such as phase-locked loops, active filters and large-signal amplifiers.

Students will use advanced RF integrated circuit simulation tools such as SpectreRF or ADS to complete homework and project assignments.

Audit Students: Students officially auditing this course are required to earn an average grade of B or higher on HW assignments and both design projects. Assignment due dates are the same schedule as the class (no exceptions). Audit students are not required to take the midterm and final exams.

Exams: There will be two major exams: a midterm and final exam. These will be closed book and closed notes. For the midterm, you are allowed to bring a single 8 ½" x 11" sheet with any information you wish on both the front and back of the page. For the final exam, you may bring no more than two 8 ½" x 11" sheets with any information you wish on both the front and back of the page.

Simulation: SPICE based circuit simulation will be used extensively in the homework and projects. Students are to use the Cadence design environment and the Spectre SPICE based circuit simulator. Course workspace will be set up for you to work on your simulations and project designs.

Design Projects: Design projects are individual projects where a circuit is designed to a set of specifications. Students are encouraged to discuss issues and ideas amongst each other, but each design must reflect the work of each individual. Project grading will come from both the *quality* and *content* of the report and the *performance of the design* against the specifications (additional details will be provided in the assignment).

Students with Disability: Reasonable accommodations will be made for students with verified disabilities. In order to take advantage of available accommodations, students must register with Disability Services for Students at 1900 Student Health Center, Campus Box 7509, 515-7653, http://www.ncsu.edu/provost/offices/affirm_action/dss. For more information on NC State's policy on working with students with disabilities, please see Appendix K of the Handbook for Advising and Teaching (http://www.ncsu.edu/provost/hat/current/index.html).

Academic Integrity: Students should refer to the University policy on academic integrity found in the Code of Student Conduct (found in Appendix L of the Handbook for Advising and Teaching). It is the instructor's understanding and expectation that the student's signature on any test or assignment means that the student neither gave nor received unauthorized aid.

Outline of **ECE792X: Integrated Circuit Design for Wireless Communications**

I. Wireless Communications
   a. Standards (Ch. 2.1 – 2.2)
   b. Quadrature Modulation (Ch 2.3, Ch 19.2.6)
   c. Path loss (2.4)
   d. Required signal to noise (SNR) to meet a specified bit error rate (BER)
   e. Thermal noise power limits on SNR

II. System Level Considerations for Receivers
   a. Transceiver architectures: direct conversion and superheterodyne (Ch 9.2.3 – 9.4)
   b. Nonlinearity, intermodulation distortion and intercept points (12.6 – 12.7)
   c. Cascaded nonlinearity and the impact of feedback on linearity
   d. Noise and noise sources (11.1 – 11.5)
   e. Noise figure (11.6)

III. Circuits with Integrated Passive Components
   a. LRC versus RC circuits
   b. LRC resonators, Q, and bandwidth (3.2)
   c. Impedance matching and maximum power transfer (3.3 – 3.5.1)
   d. Two element matching (series L shunt C, series C shunt L) Q constrained (3.5.2)
   e. Three element matching (pi and tee) element values not Q constrained (3.5.3 – 3.5.4)
   f. Integrated resistors (4.2 – 4.3)
   g. Integrated capacitors (4.4)
   h. Integrated and bondwire inductors (4.5)

IV. CMOS LNA Design (12)
   a. Common source amplifier gain and frequency response
   b. MOSFET Noise model (11.10)
   c. Low frequency noise figure with just drain and load thermal noise
   d. General two-port admittance noise parameters (12.1)
   e. Common source MOSFET linearity
   f. Source inductance: Adjust L to achieve desired real part and resonant out reactance (12.3)

V. Mixers and Frequency Conversion
   a. Conversion gain of ideal multiplier mixers with sinusoidal and square LO
   b. Double and single balanced mixers
   c. Passive mixer and band-pass subsampling mixers
   d. Image frequency and image rejection mixer
   e. Noise in mixers
   f. LO buffer circuit for driving mixer
   g. Mixer linearity

VI. Phase shifters
   a. HPF – LPF RC phase shifter
   b. Polyphase RC filters
   c. Quadrature frequency divider

VII. Transmitter circuits
   a. Transmitter architectures
   b. Class A amplifier efficiency (R and L loads)
   c. Class AB amplifier
   d. Linearity of amplifiers in wireless systems
   e. High efficiency amplifiers

VIII. Phase locked loops
   a. Integer N PLL
   b. Linearized PLL loop analysis
   c. 2nd order PLL loop for charge pump based PLL
   d. Phase detectors

IX. Oscillators
   a. Negative resistance differential oscillator
   b. Single ended Colpitts oscillator